

COMPAL CONFIDENTIAL

MODEL NAME : BAL21

PCB NO : DAZ1PJ00100 (DA6001KR000)

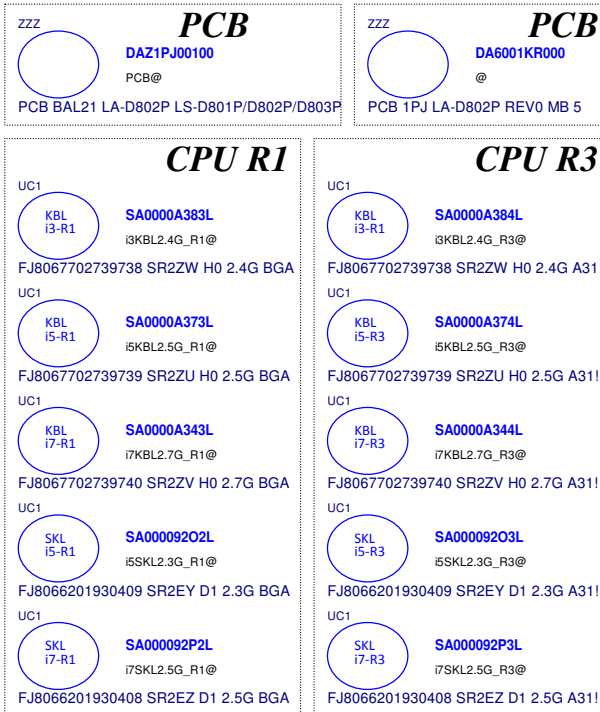
BOM P/N : 431A2Q31L01

SMT MB AD802 BAL21 KBL ES UMA

SKL-U+MEC1404 board

2016-06-21

REV : 1.0 (A00)



@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
DSX@/N_DSX@ : DSX Mode

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Nopop Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
3D@ : 3D Camera

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Layout Dell logo



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REV: X00
PWB: 9HTP8

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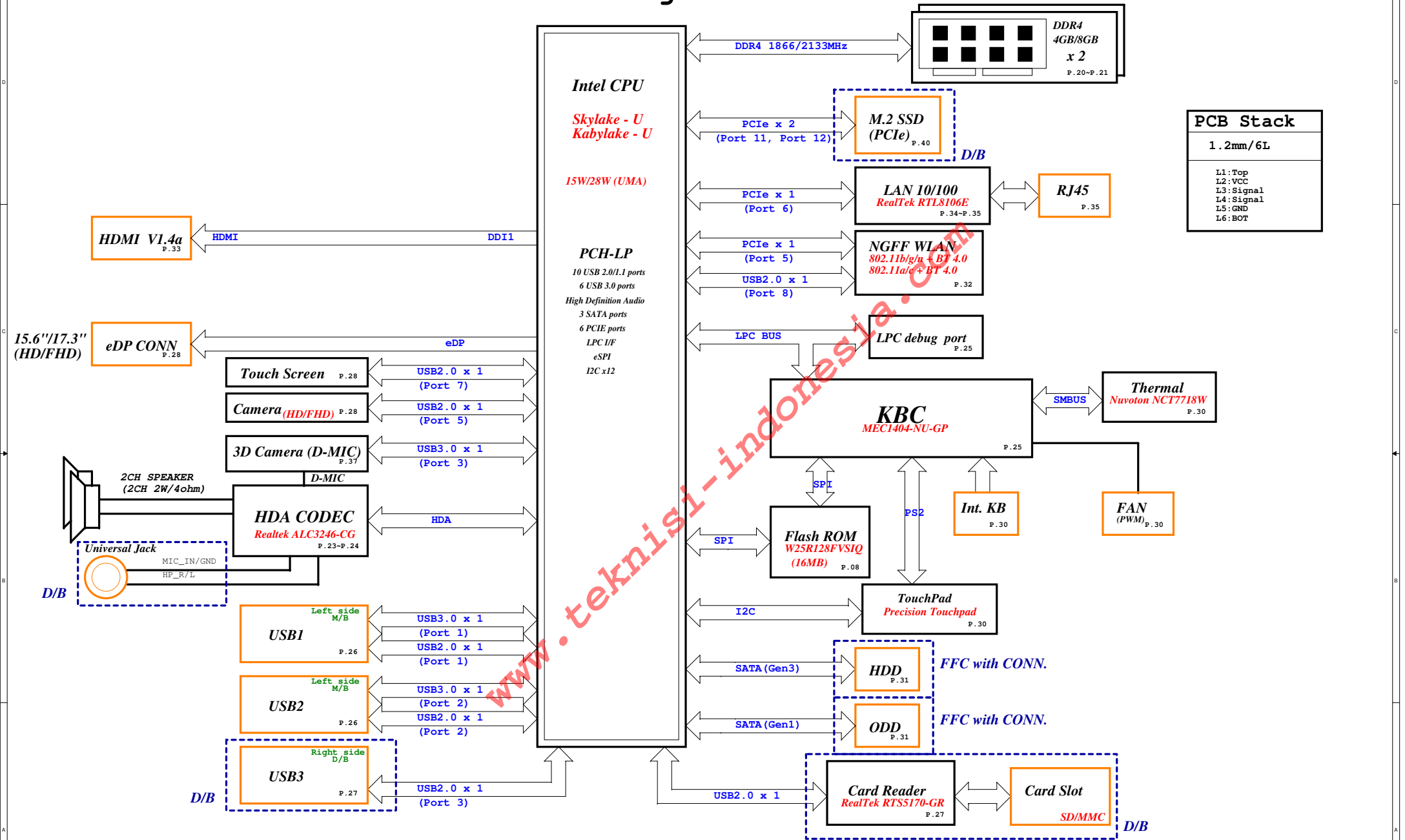
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Cover Page

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Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB3.0 Port1
2	USB3.0 Port2
3	IO/DB
4	N/A
5	CCD
6	Card Reader
7	Touch Screen
8	BT
9	N/A
10	N/A

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port1
USB3.0-2	SSIC-1			USB3.0 Port2
USB3.0-3	SSIC-2			3D Camera
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		WLAN
		PCIE-6		10/100M LAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	SATA ODD
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	N/A

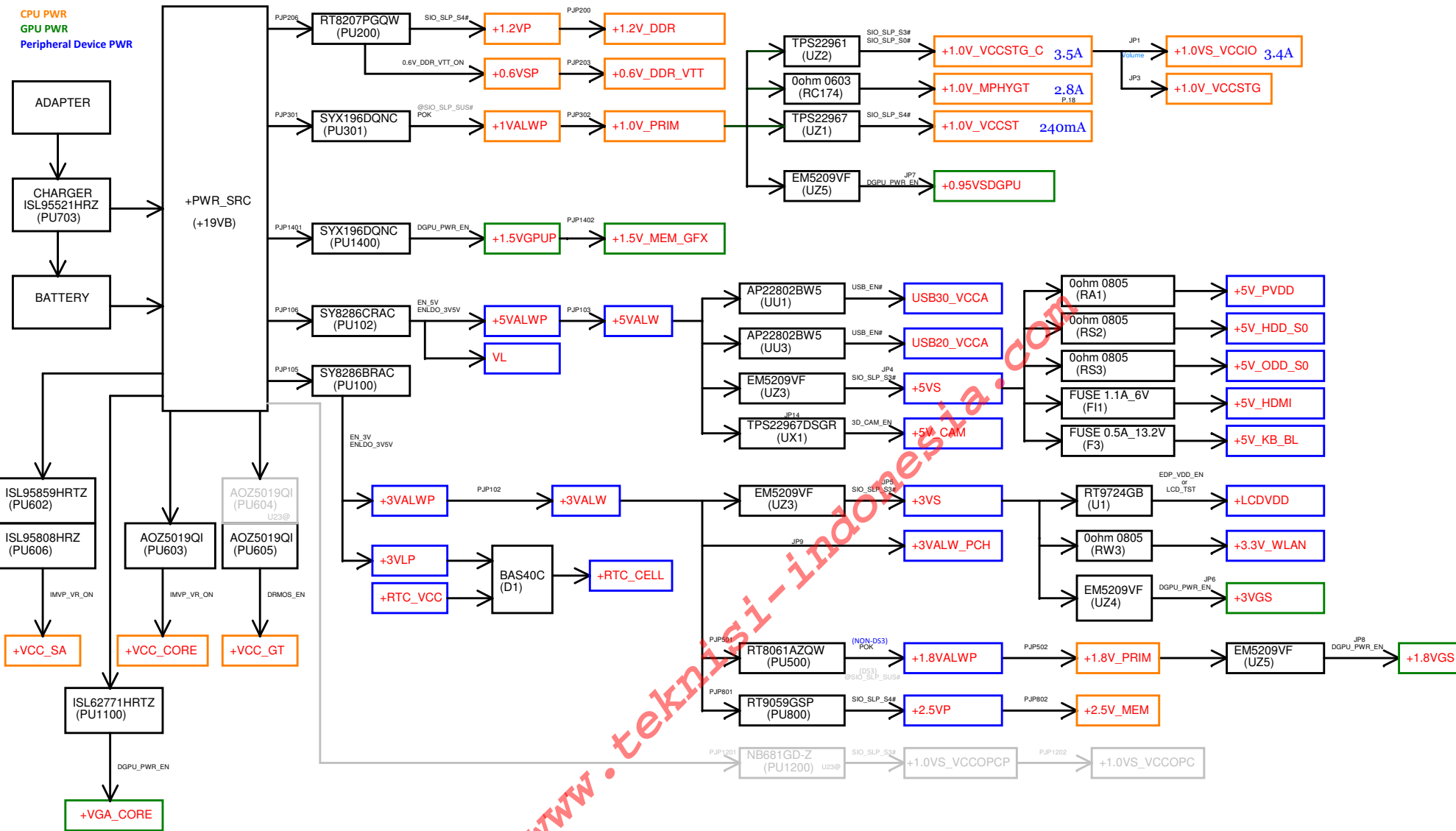
PM TABLE

power plane State	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VGA_CORE +VCC_CORE +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT
2	100	13.7	2.902	DVT1
3	100	17.8	2.801	DVT2
4	100	22.1	2.703	
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	

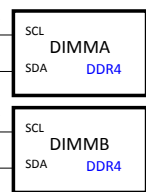
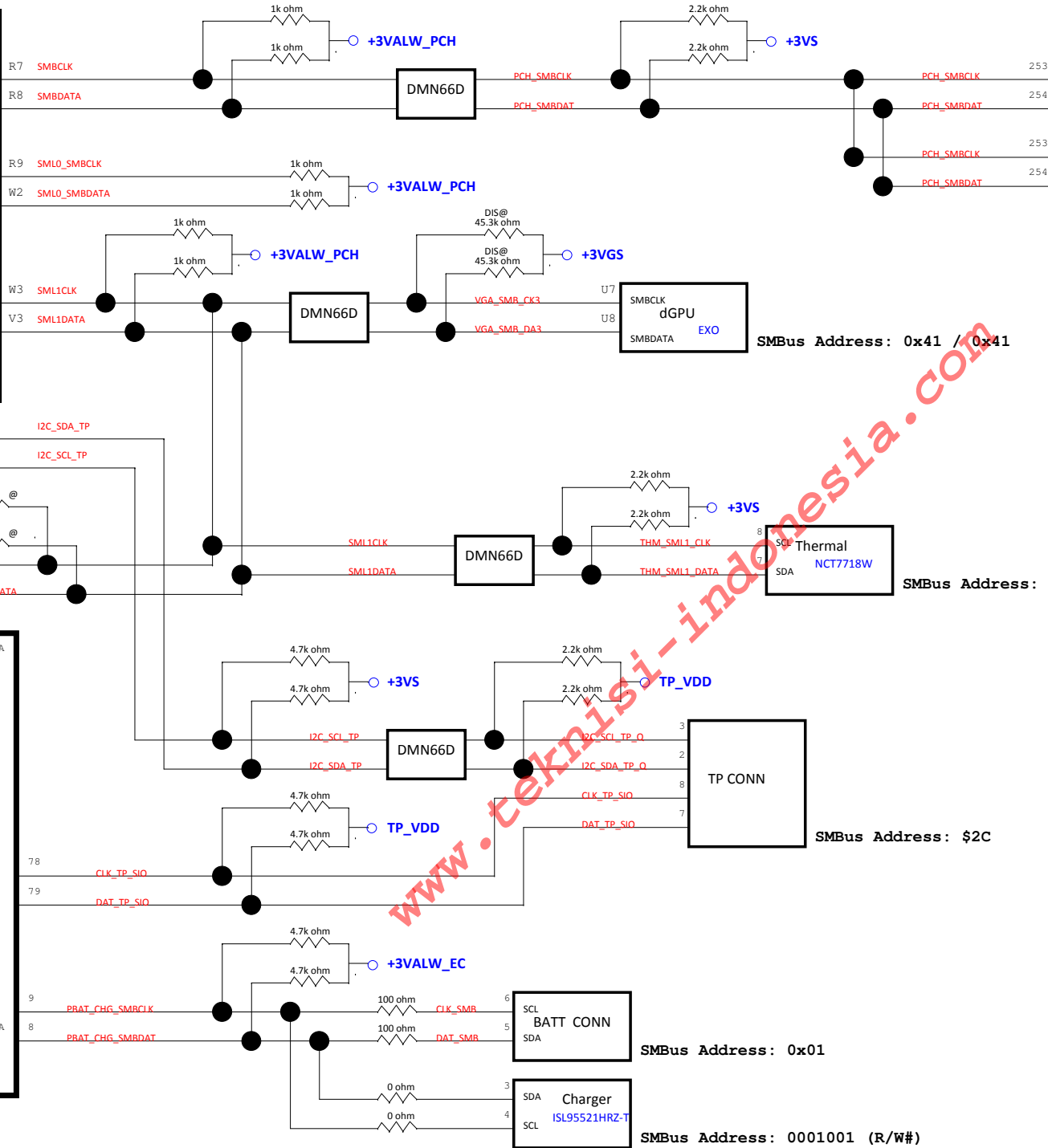
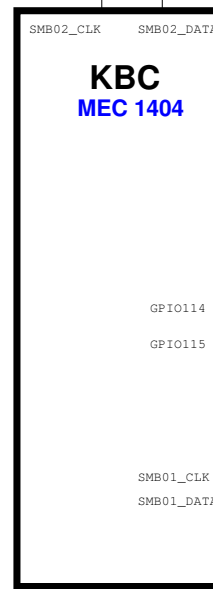
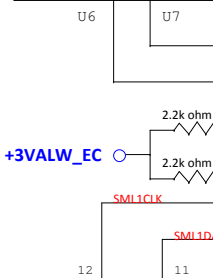
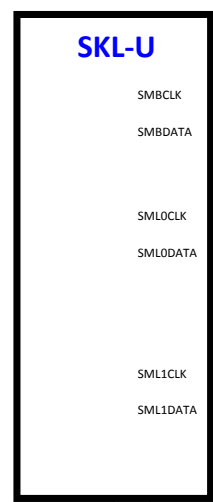
CPU PWR
GPU PWR
Peripheral Device PWR



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SMBus Address: 000

SMBus Address: 010

SMBus Address: 0x41 / 0x41

SMBus Address: 1001100xb (x is R/W bit)

SMBus Address: \$2C

SMBus Address: 0x01

SMBus Address: 0001001 (R/W#)

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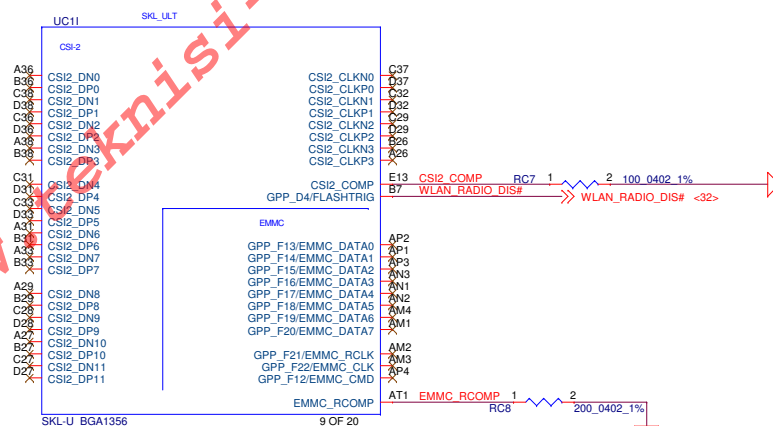
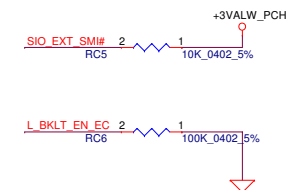
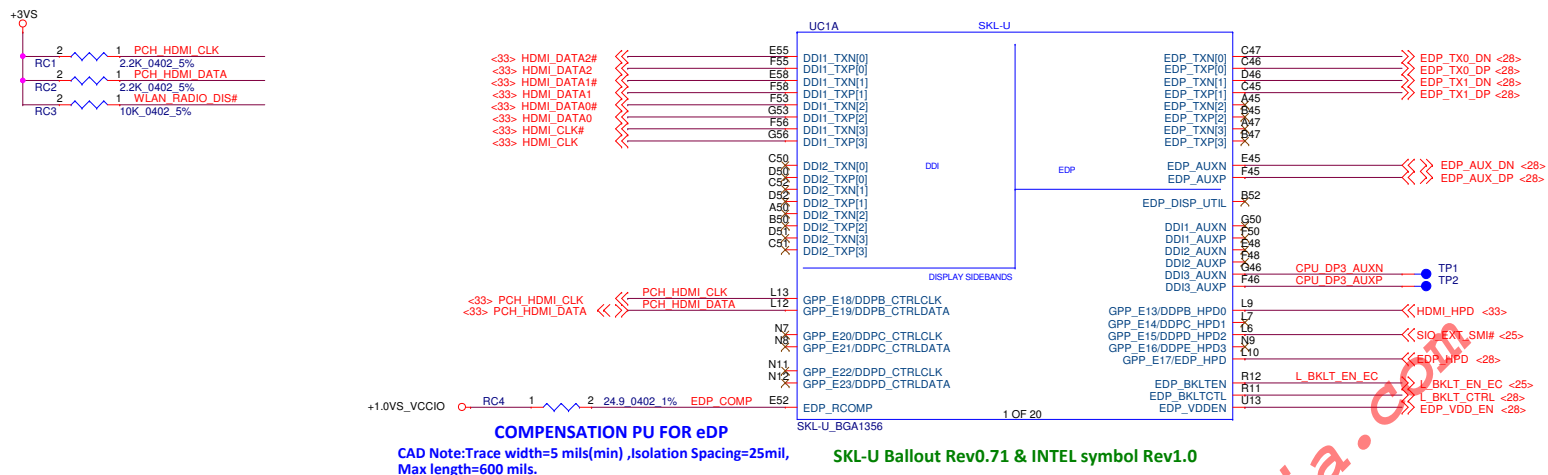
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SMBus Block diagram

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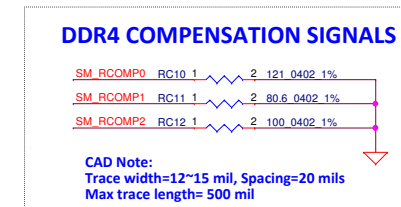
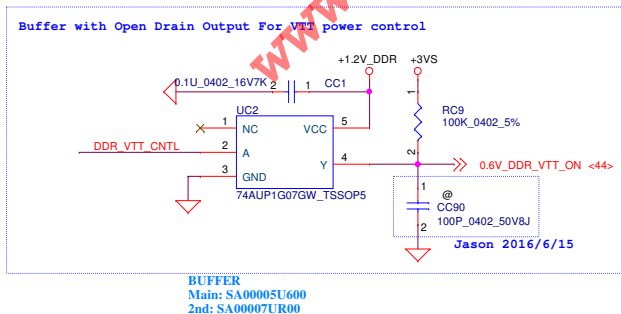
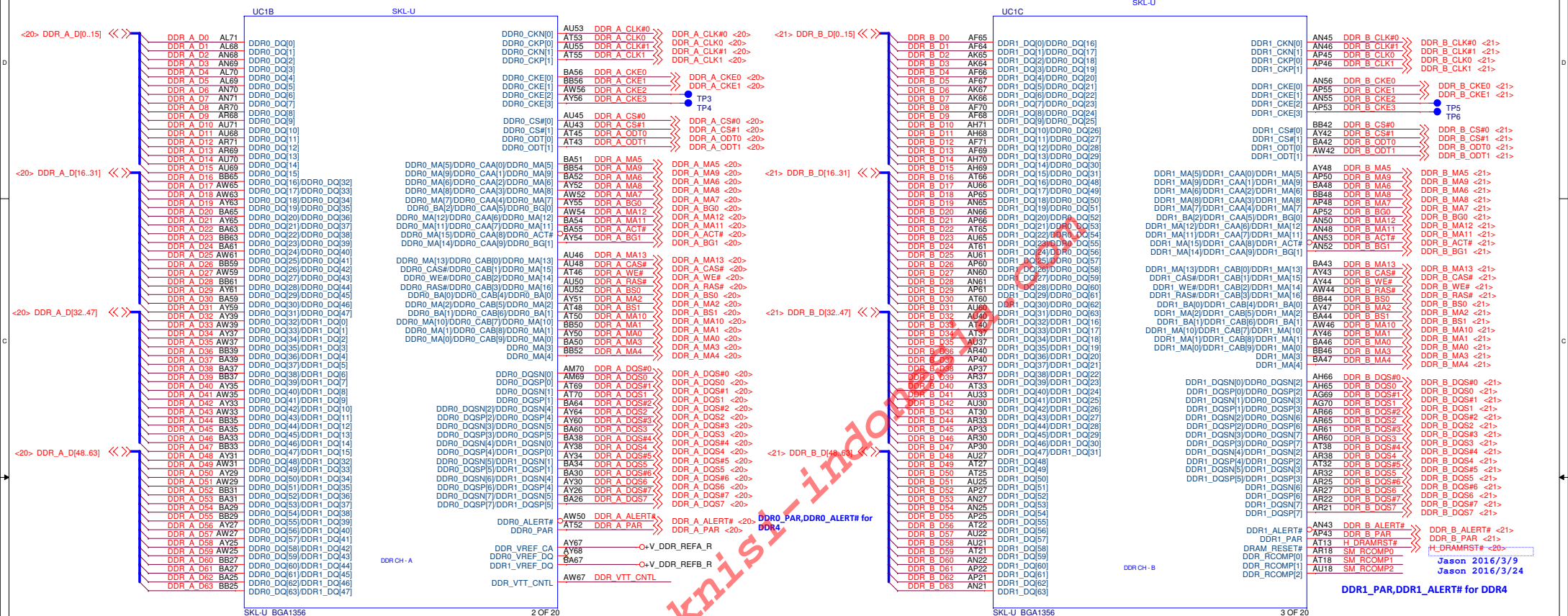
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DDR4 Interleaved Memory



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Title **MCP(2/14)DDR4**

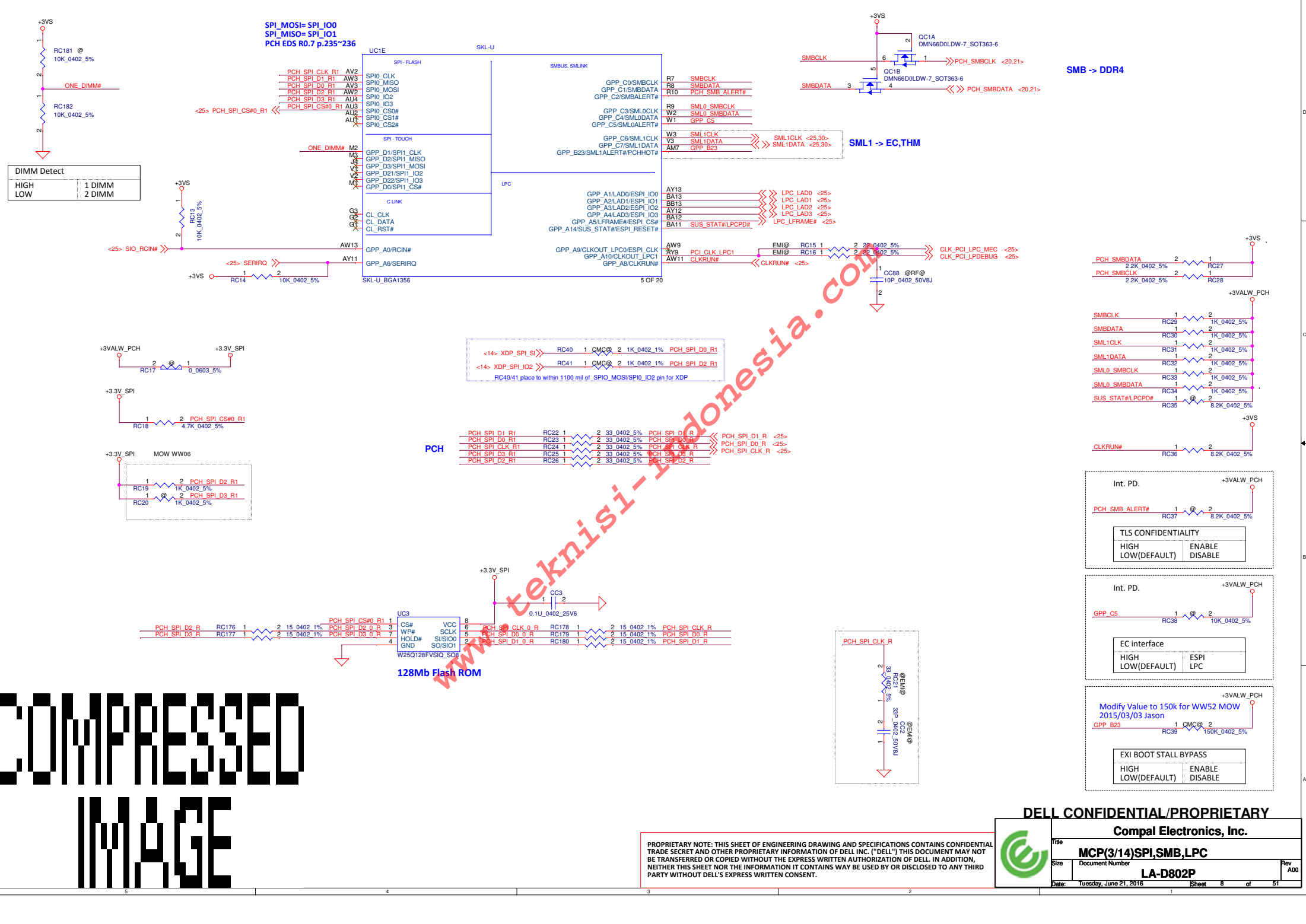
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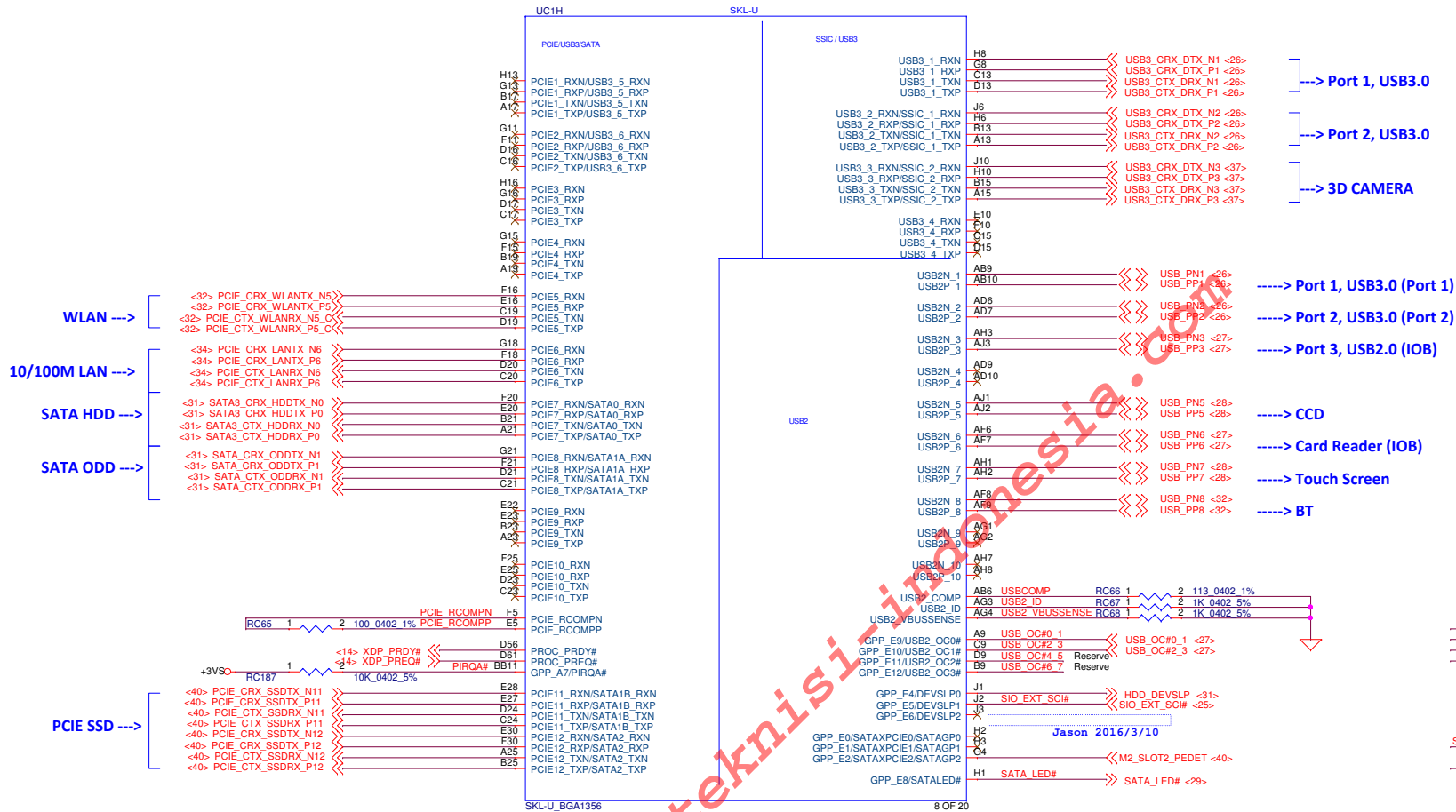
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IMAGE



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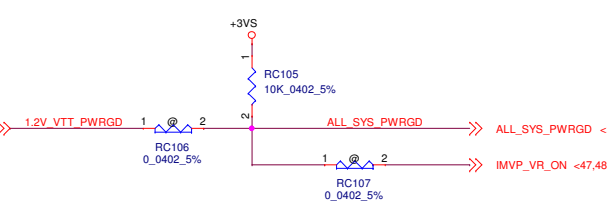
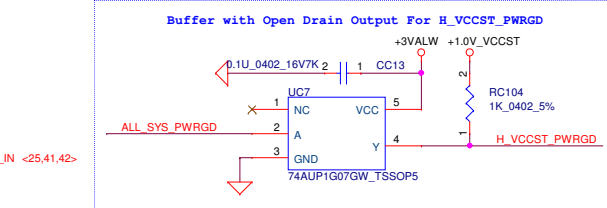
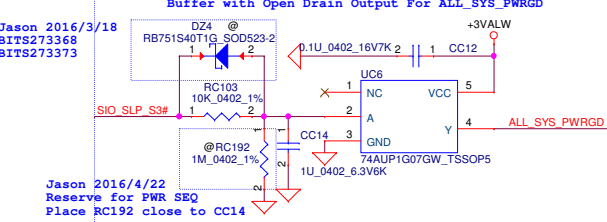
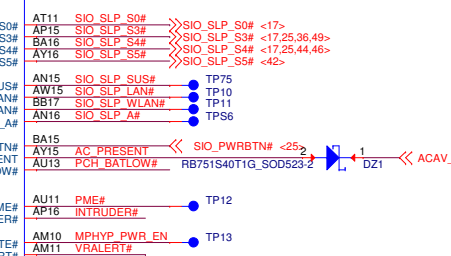
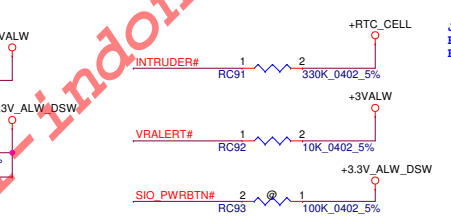
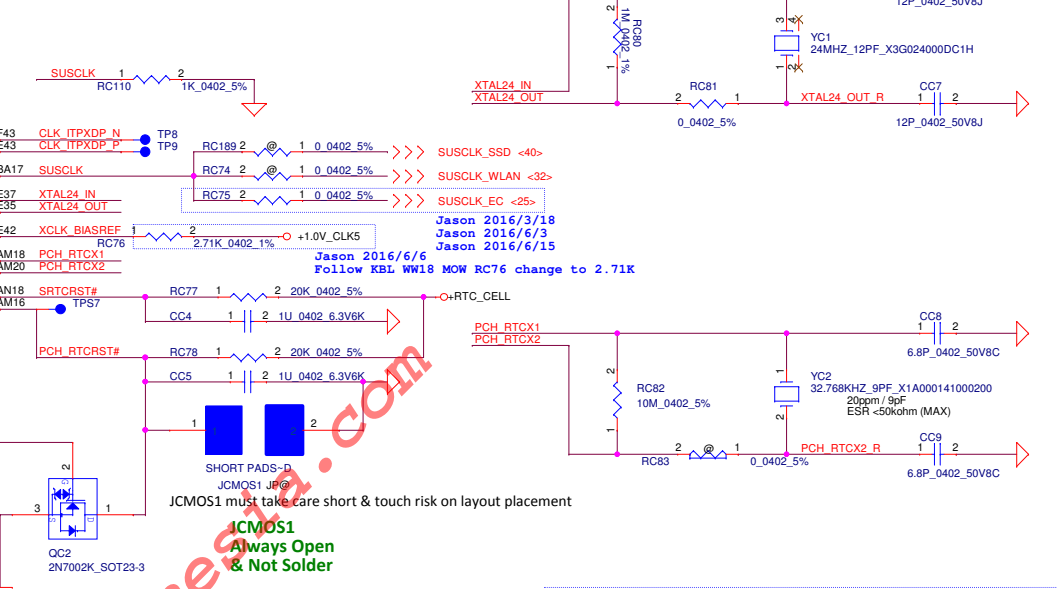
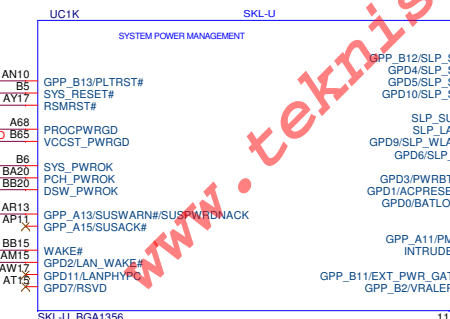
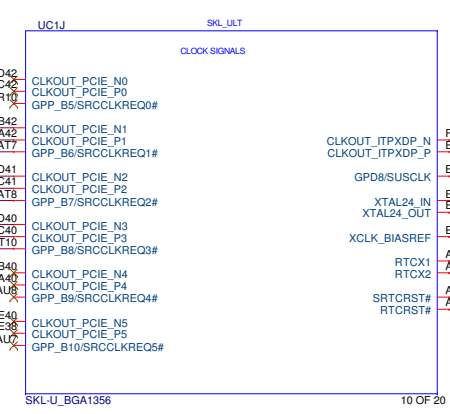
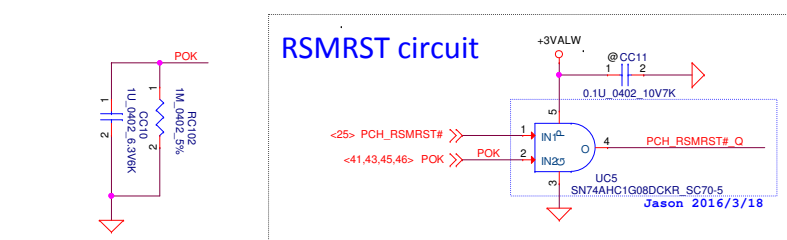
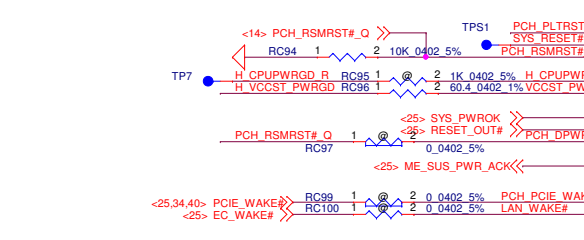
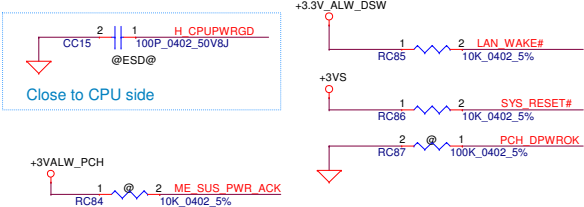
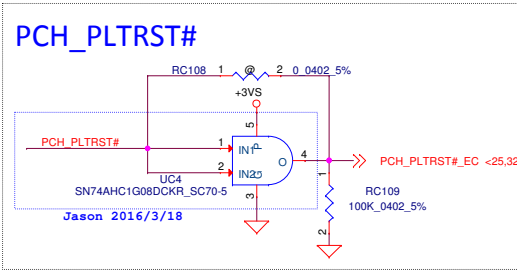
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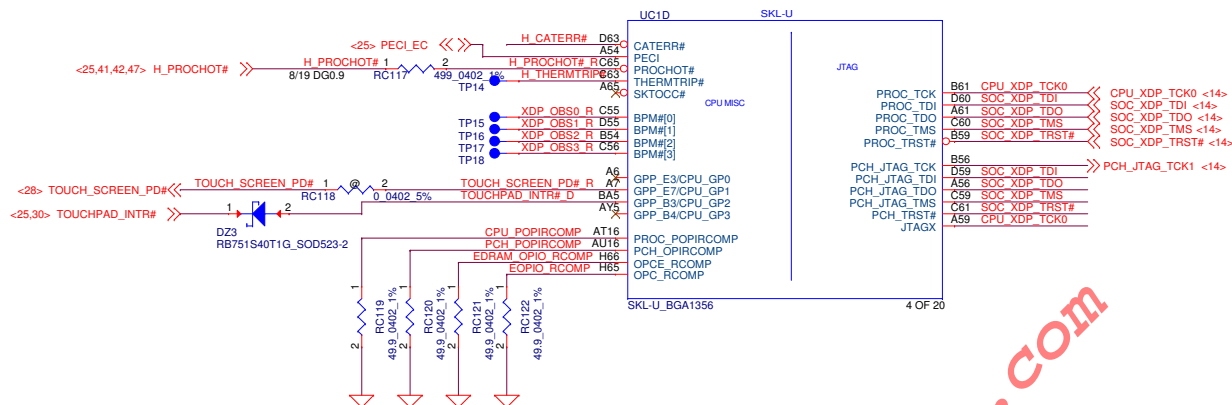
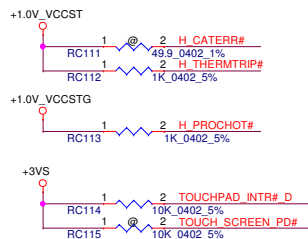
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Title		MCP(5/14)PCIE,USB,SATA	
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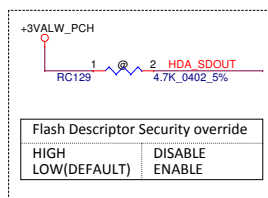
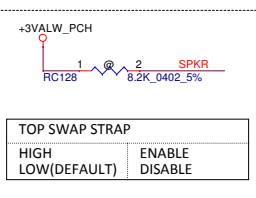
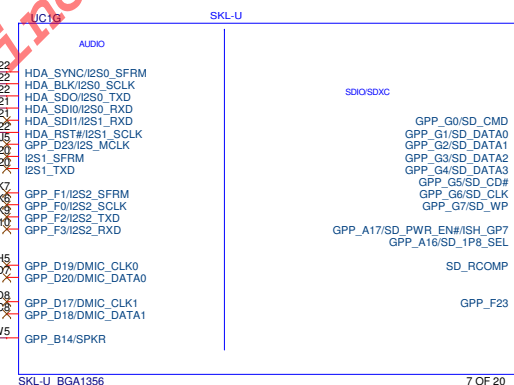
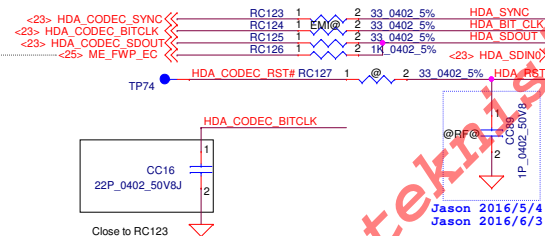
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ME_FWP_EC

- LOW = ENABLE -->ME lock, can't update ME
- HIGH = DISABLE -->ME un-lock, can update ME



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Title MCP(7/14)MISC,JTAG,HDA,SDIO

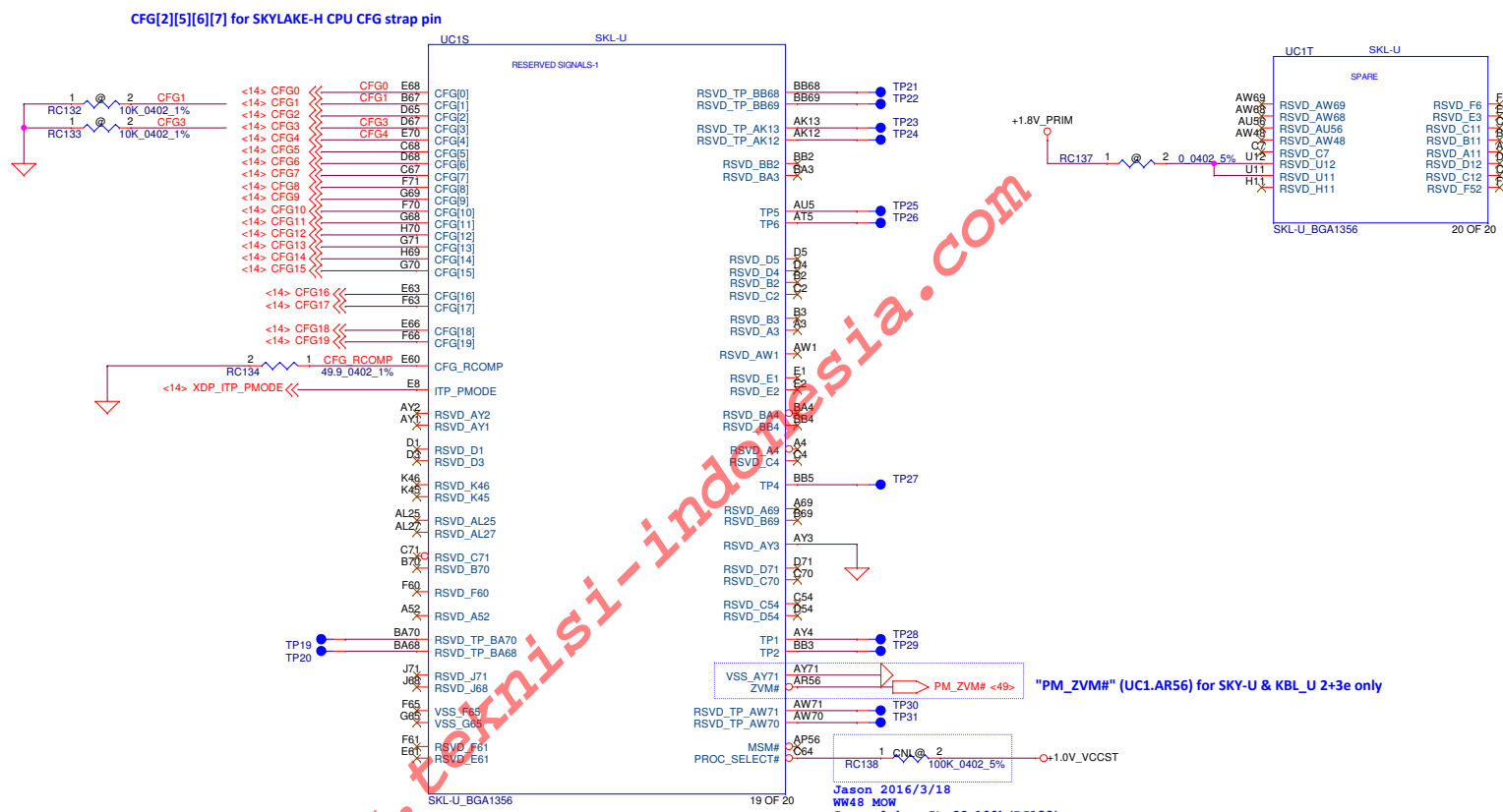
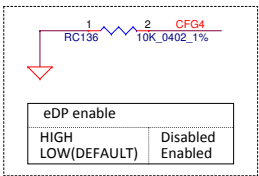
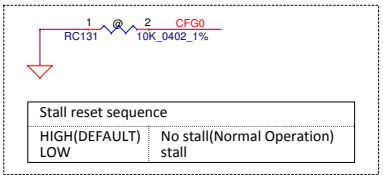
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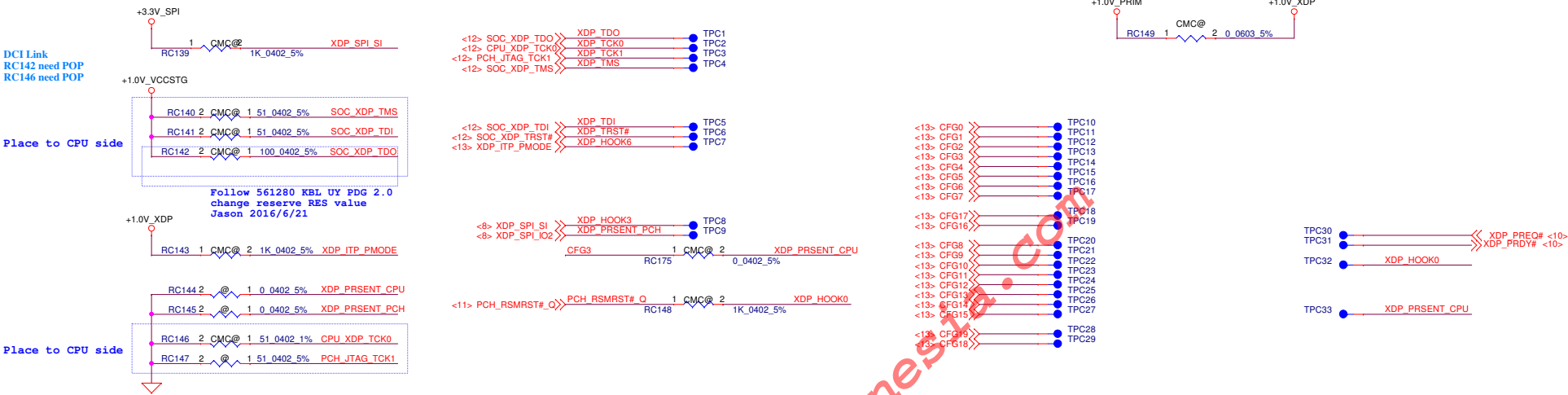
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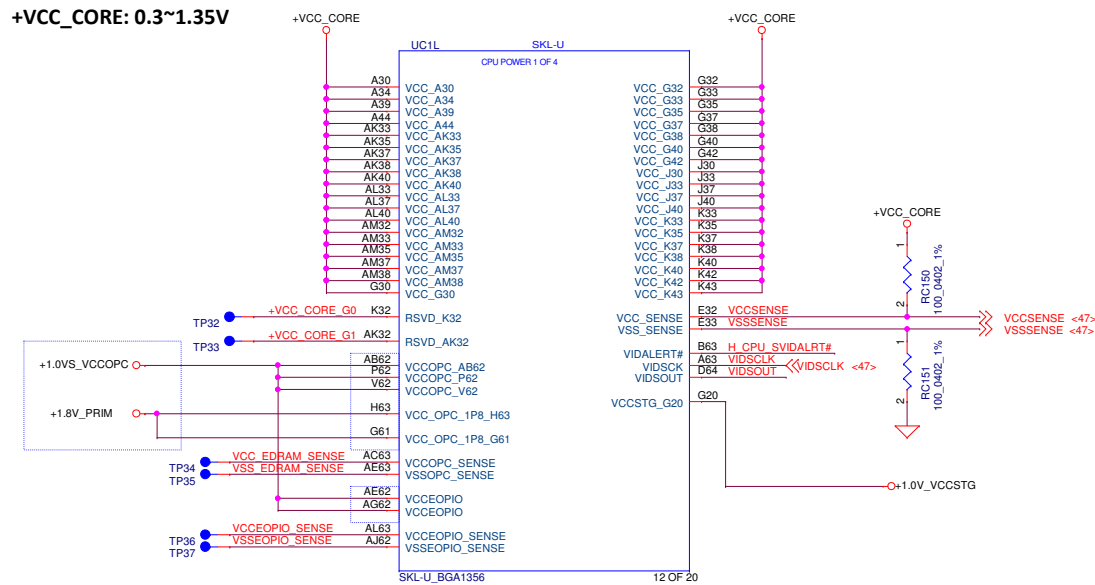
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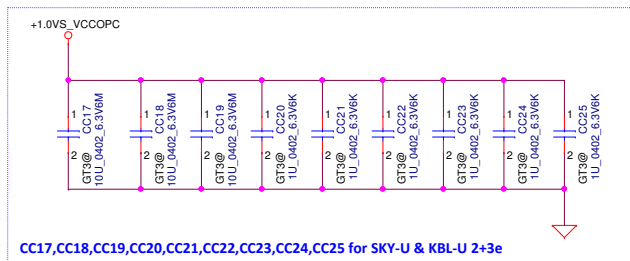
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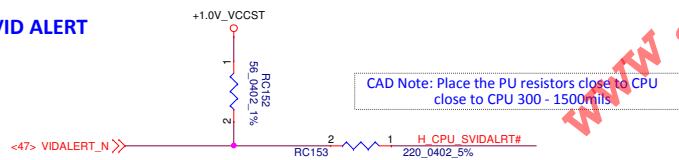
+VCC_CORE: 0.3~1.35V



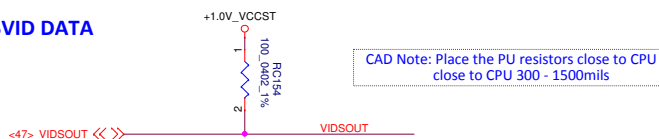
VCCOPC, VCCOPC_1P8, VCCEOPIO for SKYLAKE-U 2+3e (w/ on package cache)



SVID ALERT



SVID DATA



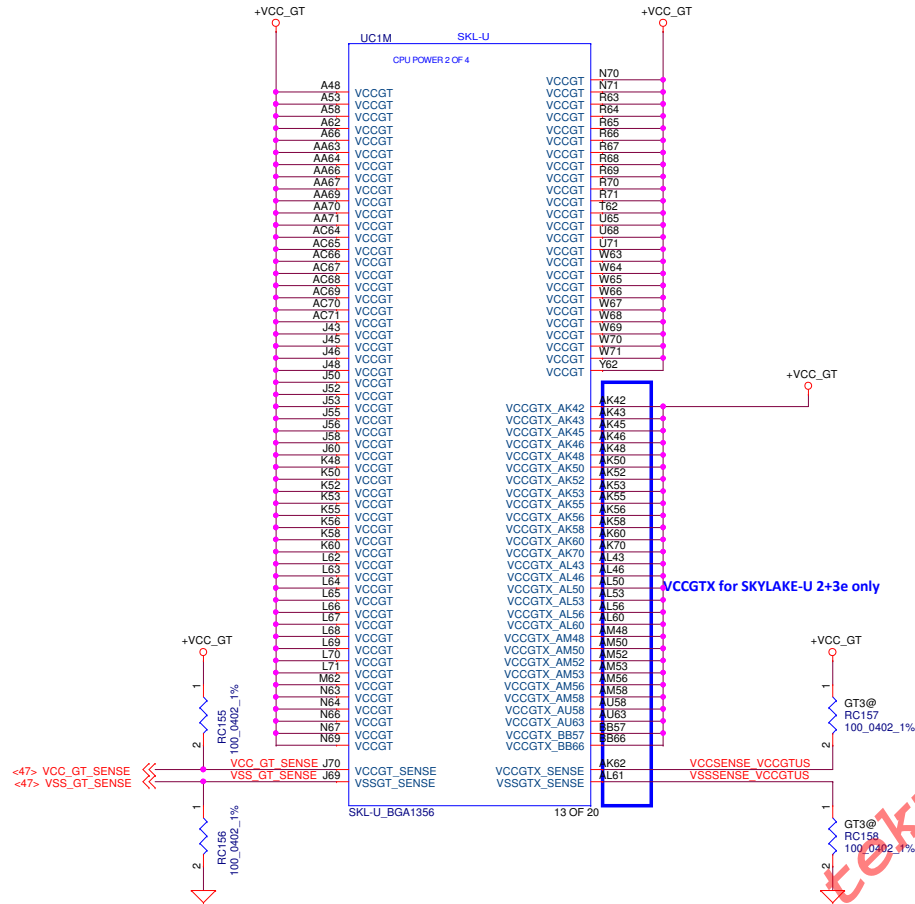
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Power source

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MCP(10/14)PWR-VCC CORE			
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+VCCGT: 0.3~1.35V
+VCCGTx : 0.3~1.35V



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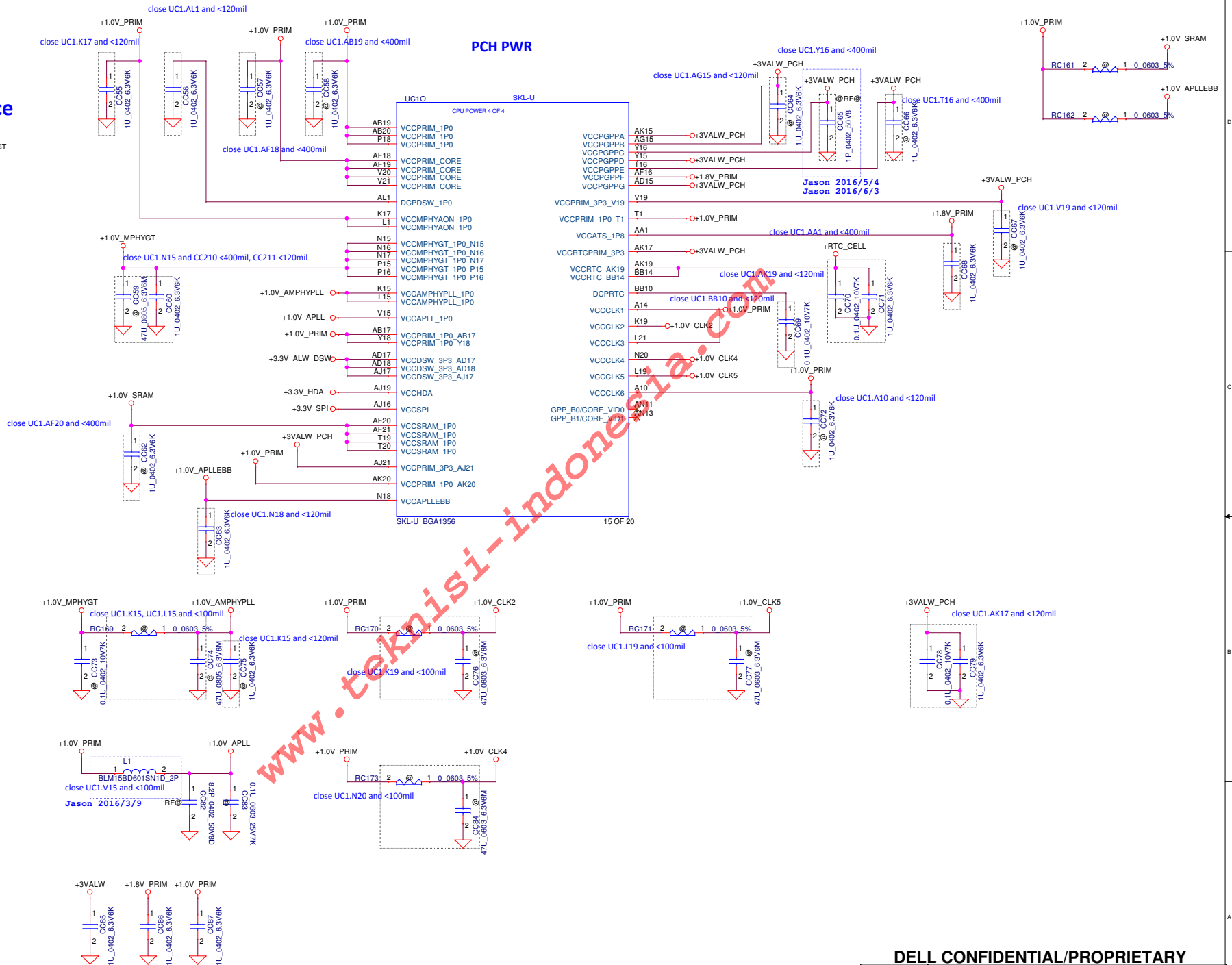
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+1.0V_PRIM +1.0V_MPHYGT



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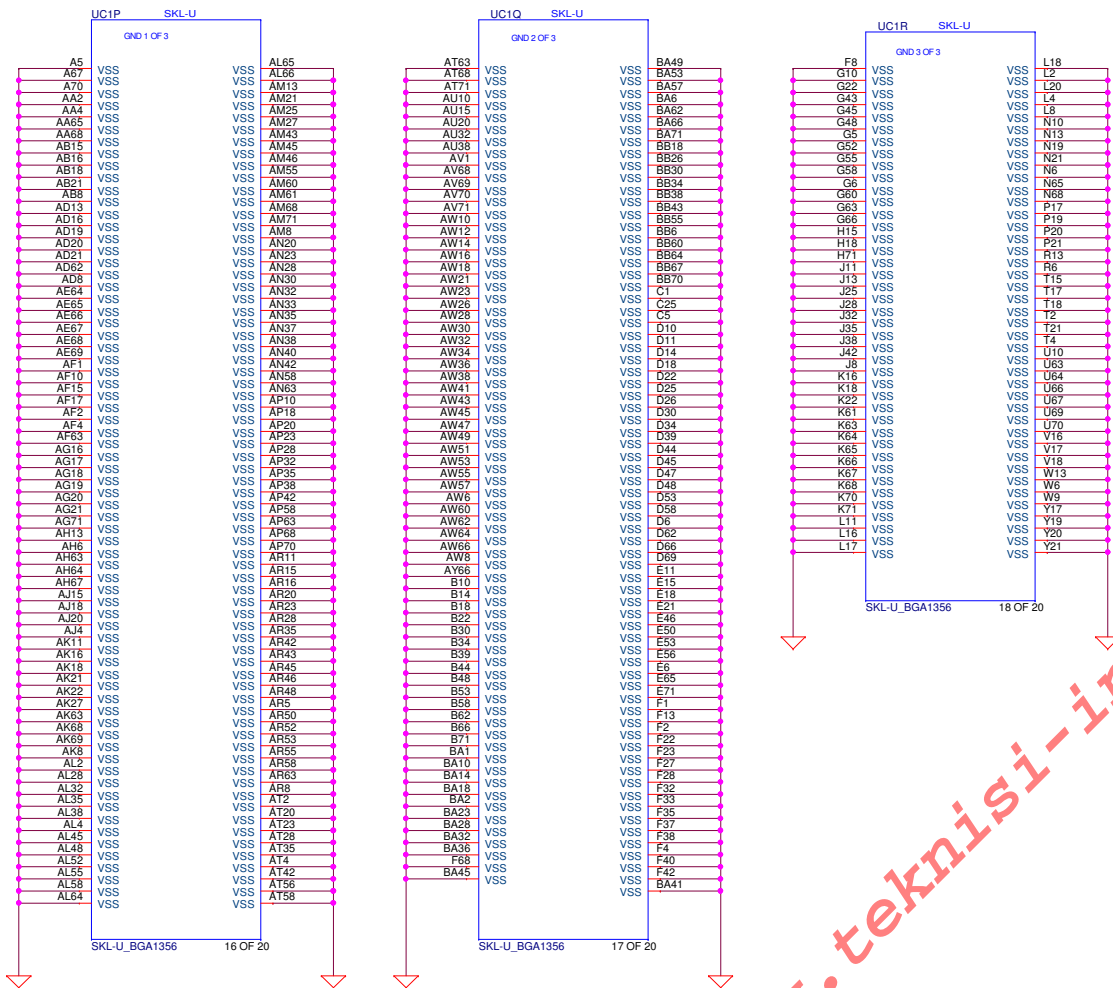


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IMAGE


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Title			MCP(14/14)VSS	
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The diagram illustrates a 12V power distribution system for a Raspberry Pi 3B+. It features two +1.2V_DDR power rails, each connected to a 5-pin header. The top rail is connected to pins 1 through 5, which are labeled CU18 through CU14. The bottom rail is connected to pins 1 through 5, which are labeled CU26 through CU22. A 3.3V regulator is shown on the right, connected to the 3.3V pin of the header and ground. The regulator is labeled CU27 and has a 330U_D2_2V_Y output. The diagram is dated Jason 2016/3/9 and Jason 2016/3/1.

[illegible]

Timing diagram showing the relationship between `DDR4_DRAMRST*` and `H_DRAMRST*` signals. The diagram includes a red arrow pointing to the falling edge of `DDR4_DRAMRST*` with the text "Don't POP for KBL". A blue arrow points to the rising edge of `H_DRAMRST*` with the text "Jason 2016/3/24". The diagram also shows a 0.0402 5% resistor and a 0.10 0.0402 807A capacitor. The signal levels are +2.0V and +1.2V.

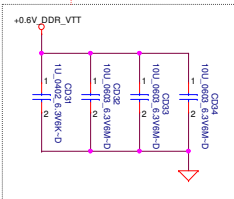
Jason 2016/3/24

Figure 10-10 shows the pin connections for the i.MX8M Mini module. The diagram is a detailed pinout for the i.MX8M Mini module, showing the connections for the +1.2V_DDR, +1.2V_DDR, +1.2V_DDR, and +1.2V_DDR power planes. The pinout is organized into columns, with the left side showing the module pins and the right side showing the board pins. The module pins are labeled with their functions, such as DDR_A D1, DDR_A D5, DDR_A D9, DDR_A D13, DDR_A D17, DDR_A D21, DDR_A D25, DDR_A D29, DDR_A D33, DDR_A D37, DDR_A D41, DDR_A D45, DDR_A D49, DDR_A D53, DDR_A D57, DDR_A D61, DDR_A D65, DDR_A D69, DDR_A D73, DDR_A D77, DDR_A D81, DDR_A D85, DDR_A D89, DDR_A D93, DDR_A D97, DDR_A D101, DDR_A D105, DDR_A D109, DDR_A D113, DDR_A D117, DDR_A D121, DDR_A D125, DDR_A D129, DDR_A D133, DDR_A D137, DDR_A D141, DDR_A D145, DDR_A D149, DDR_A D153, DDR_A D157, DDR_A D161, DDR_A D165, DDR_A D169, DDR_A D173, DDR_A D177, DDR_A D181, DDR_A D185, DDR_A D189, DDR_A D193, DDR_A D197, DDR_A D201, DDR_A D205, DDR_A D209, DDR_A D213, DDR_A D217, DDR_A D221, DDR_A D225, DDR_A D229, DDR_A D233, DDR_A D237, DDR_A D241, DDR_A D245, DDR_A D249, DDR_A D253, DDR_A D257, DDR_A D261, DDR_A D265, DDR_A D269, DDR_A D273, DDR_A D277, DDR_A D281, DDR_A D285, DDR_A D289, DDR_A D293, DDR_A D297, DDR_A D301, DDR_A D305, DDR_A D309, DDR_A D313, DDR_A D317, DDR_A D321, DDR_A D325, DDR_A D329, DDR_A D333, DDR_A D337, DDR_A D341, DDR_A D345, DDR_A D349, DDR_A D353, DDR_A D357, DDR_A D361, DDR_A D365, DDR_A D369, DDR_A D373, DDR_A D377, DDR_A D381, DDR_A D385, DDR_A D389, DDR_A D393, DDR_A D397, DDR_A D401, DDR_A D405, DDR_A D409, DDR_A D413, DDR_A D417, DDR_A D421, DDR_A D425, DDR_A D429, DDR_A D433, DDR_A D437, DDR_A D441, DDR_A D445, DDR_A D449, DDR_A D453, DDR_A D457, DDR_A D461, DDR_A D465, DDR_A D469, DDR_A D473, DDR_A D477, DDR_A D481, DDR_A D485, DDR_A D489, DDR_A D493, DDR_A D497, DDR_A D501, DDR_A D505, DDR_A D509, DDR_A D513, DDR_A D517, DDR_A D521, DDR_A D525, DDR_A D529, DDR_A D533, DDR_A D537, DDR_A D541, DDR_A D545, DDR_A D549, DDR_A D553, DDR_A D557, DDR_A D561, DDR_A D565, DDR_A D569, DDR_A D573, DDR_A D577, DDR_A D581, DDR_A D585, DDR_A D589, DDR_A D593, DDR_A D597, DDR_A D601, DDR_A D605, DDR_A D609, DDR_A D613, DDR_A D617, DDR_A D621, DDR_A D625, DDR_A D629, DDR_A D633, DDR_A D637, DDR_A D641, DDR_A D645, DDR_A D649, DDR_A D653, DDR_A D657, DDR_A D661, DDR_A D665, DDR_A D669, DDR_A D673, DDR_A D677, DDR_A D681, DDR_A D685, DDR_A D689, DDR_A D693, DDR_A D697, DDR_A D701, DDR_A D705, DDR_A D709, DDR_A D713, DDR_A D717, DDR_A D721, DDR_A D725, DDR_A D729, DDR_A D733, DDR_A D737, DDR_A D741, DDR_A D745, DDR_A D749, DDR_A D753, DDR_A D757, DDR_A D761, DDR_A D765, DDR_A D769, DDR_A D773, DDR_A D777, DDR_A D781, DDR_A D785, DDR_A D789, DDR_A D793, DDR_A D797, DDR_A D801, DDR_A D805, DDR_A D809, DDR_A D813, DDR_A D817, DDR_A D821, DDR_A D825, DDR_A D829, DDR_A D833, DDR_A D837, DDR_A D841, DDR_A D845, DDR_A D849, DDR_A D853, DDR_A D857, DDR_A D861, DDR_A D865, DDR_A D869, DDR_A D873, DDR_A D877, DDR_A D881, DDR_A D885, DDR_A D889, DDR_A D893, DDR_A D897, DDR_A D901, DDR_A D905, DDR_A D909, DDR_A D913, DDR_A D917, DDR_A D921, DDR_A D925, DDR_A D929, DDR_A D933, DDR_A D937, DDR_A D941, DDR_A D945, DDR_A D949, DDR_A D953, DDR_A D957, DDR_A D961, DDR_A D965, DDR_A D969, DDR_A D973, DDR_A D977, DDR_A D981, DDR_A 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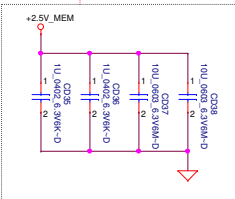
All VREF traces should have 10 mil trace width

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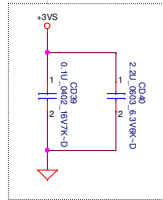
Layout Note:
Place near JDIMM2.258



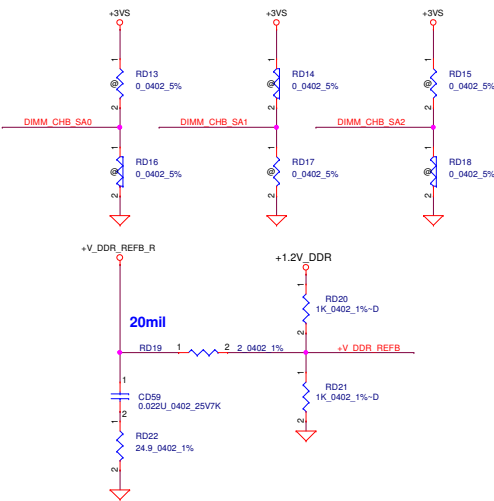
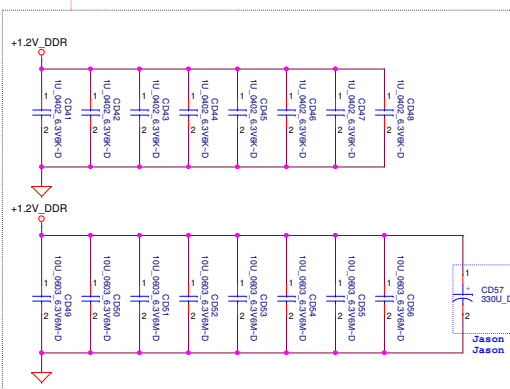
Layout Note:
Place near JDIMM2.257,259



Layout Note:
Place near JDIMM2.255



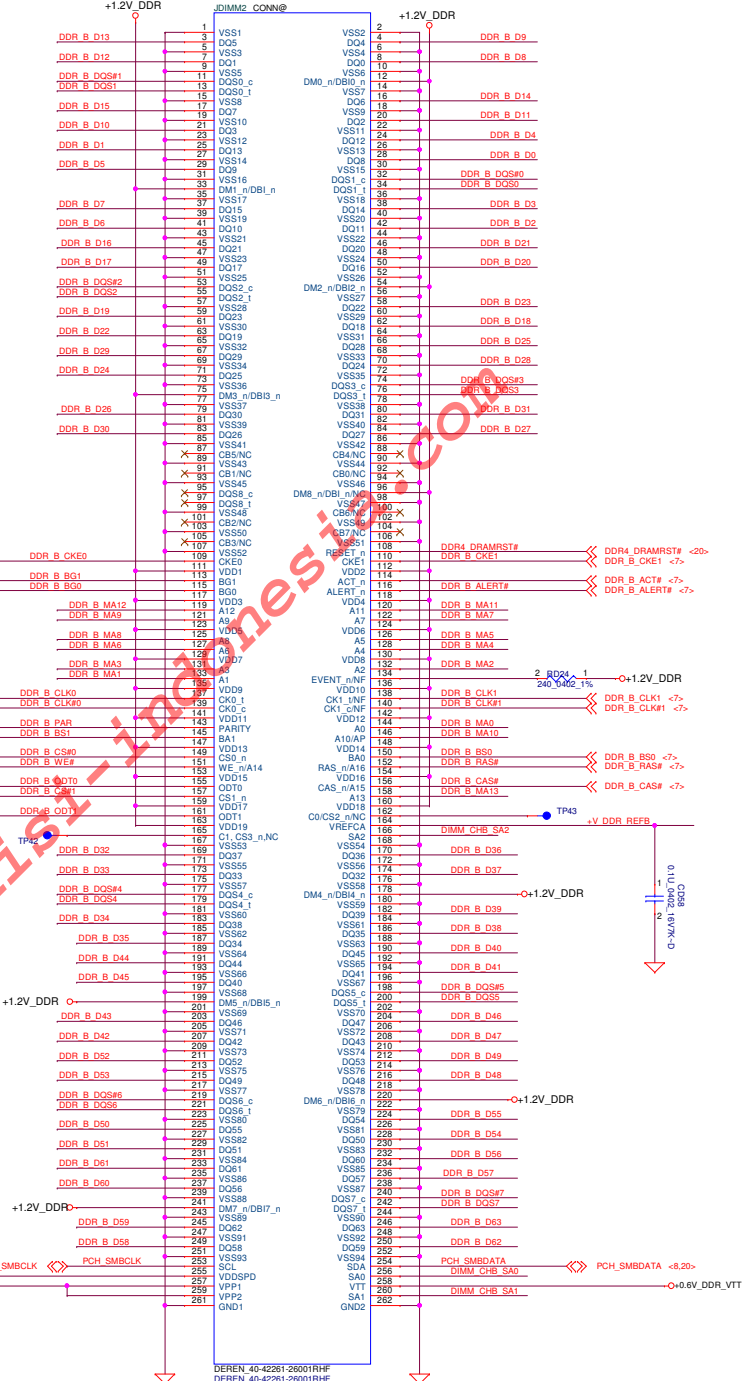
Layout Note:
Place near JDIMM2



<7> DDR_B_D10.83
<7> DDR_B_MA0.13
<7> DDR_B_DQS#0.7
<7> DDR_B_DQS#0.7



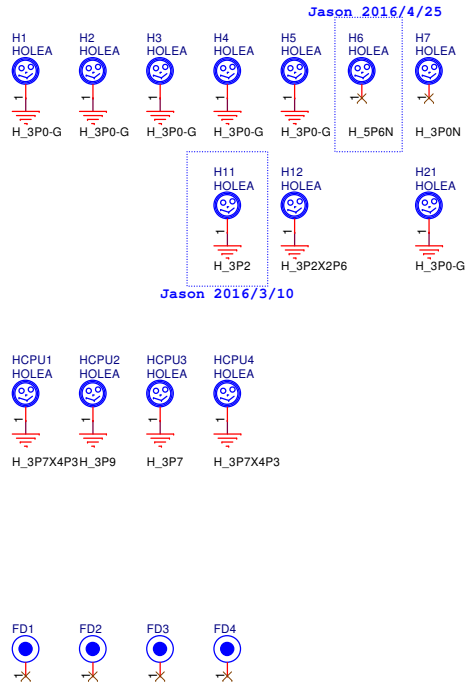
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<7> DDR_B_BG1
<7> DDR_B_BG0
<7> DDR_B_CK0
<7> DDR_B_CLK#
<7> DDR_B_PAR
<7> DDR_B_BSI
<7> DDR_B_CSA0
<7> DDR_B_WEF
<7> DDR_B_CSD0
<7> DDR_B_CSA1
<7> DDR_B_CDT1



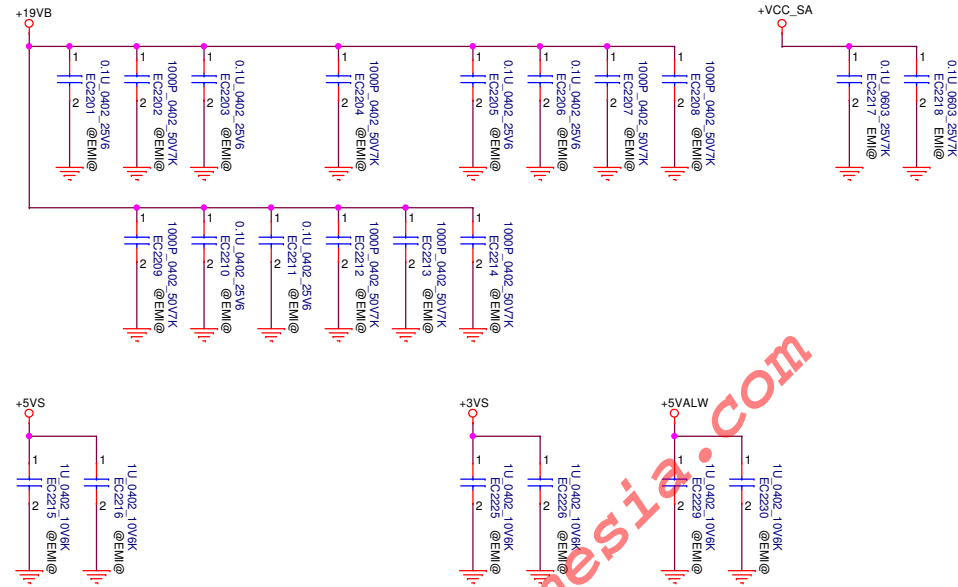
All VREF traces should
have 10 mil trace width

Main Func = Other

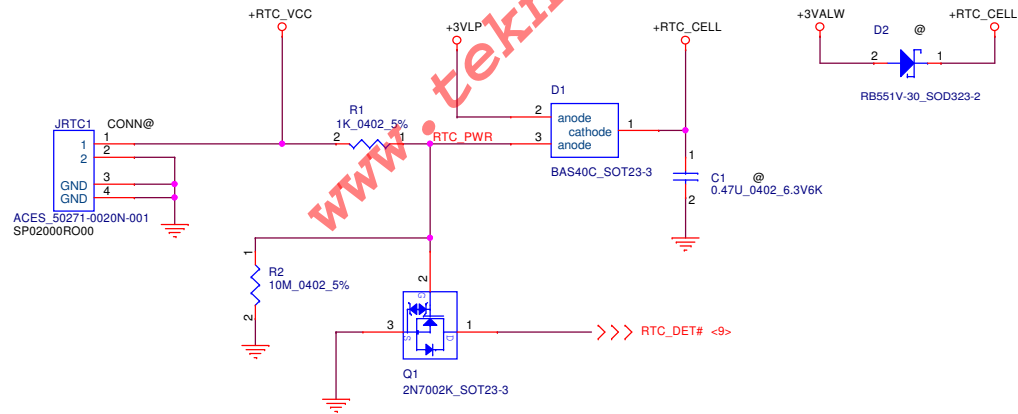
Screw hole/FD



Mind the voltage rating of the caps.

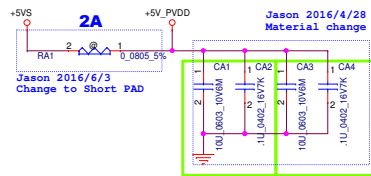


Main Func = RTC



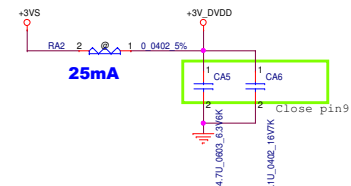
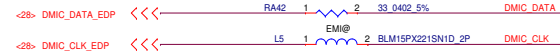
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Main Func = Audio

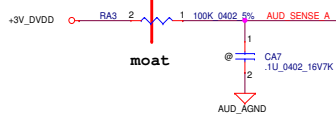


Layout Note:
Close pin41

Layout Note:
Close pin46

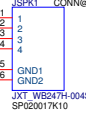
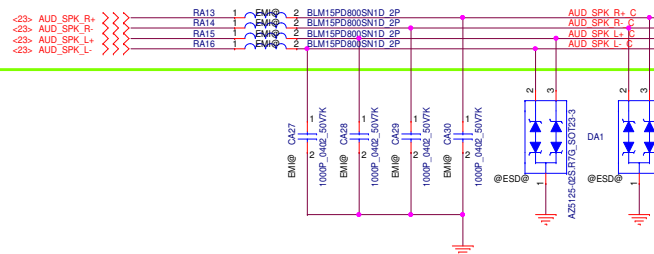


Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

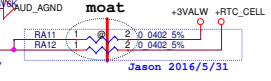
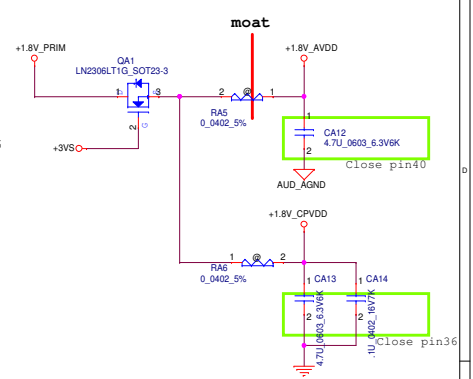
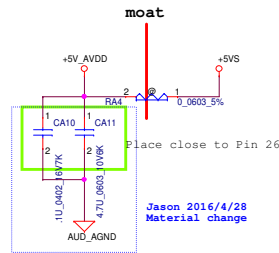
Speaker



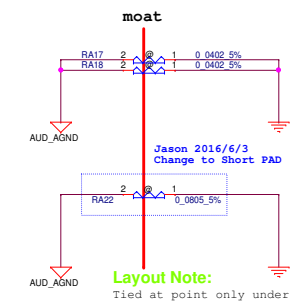
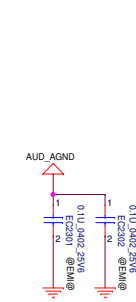
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Place on the moat between GND & GNDA.

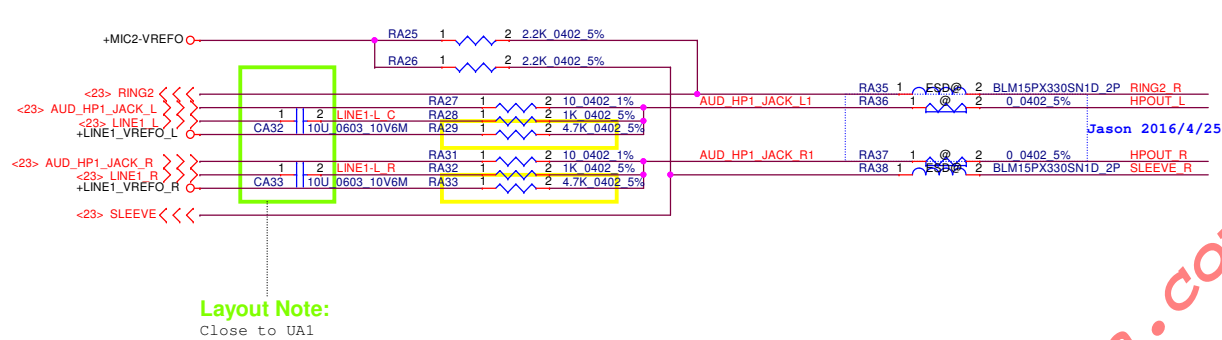


Layout Note:
Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

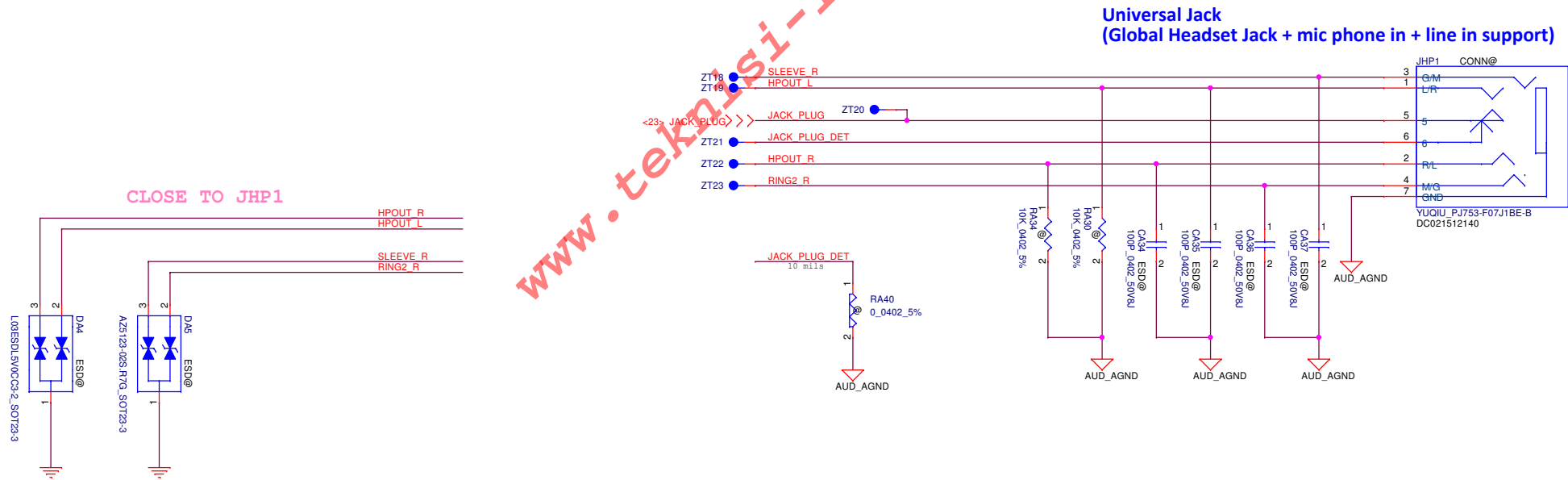


Layout Note:
Tied at point only under
Codec or near the Codec

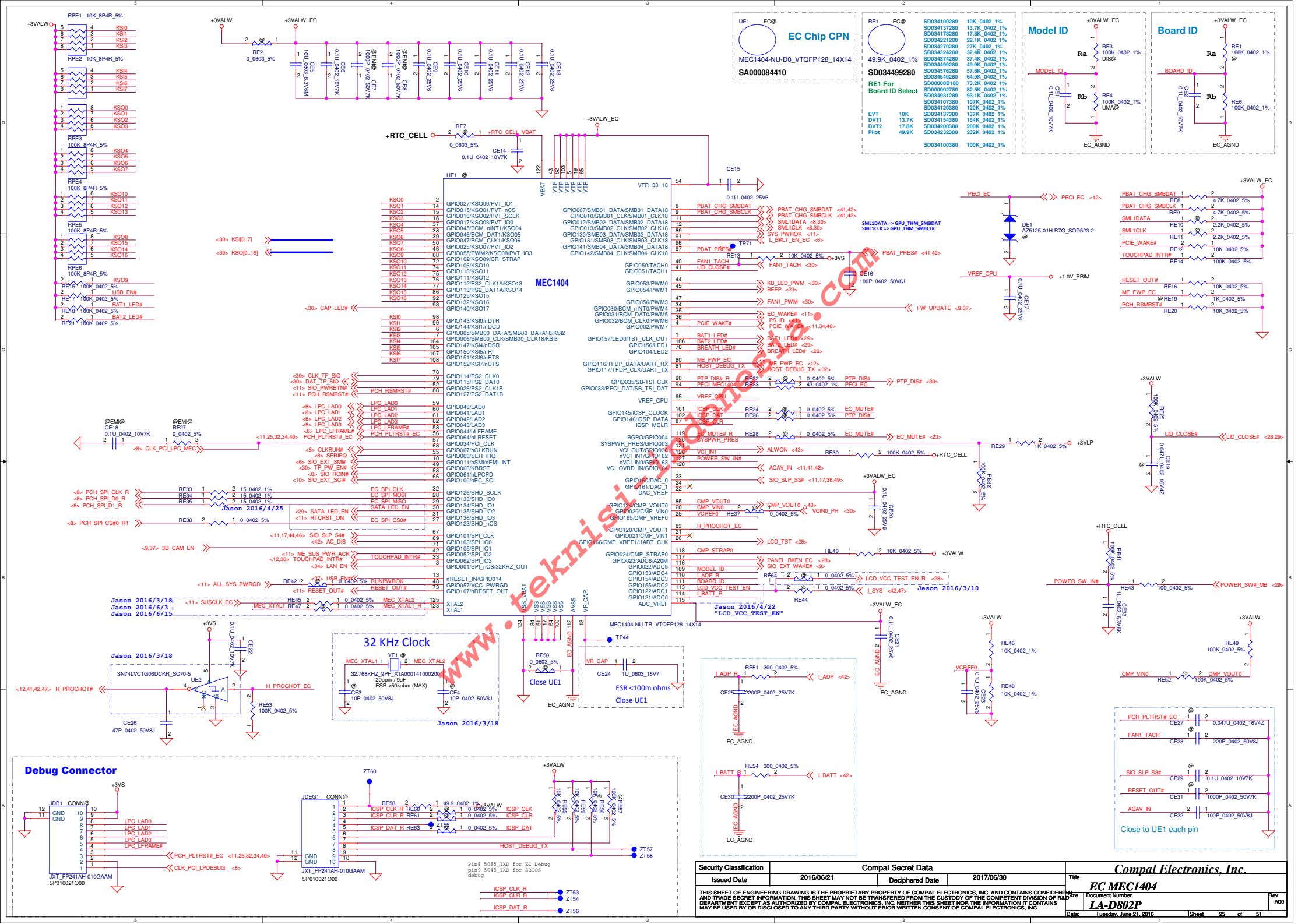
Main Func = Audio Jack



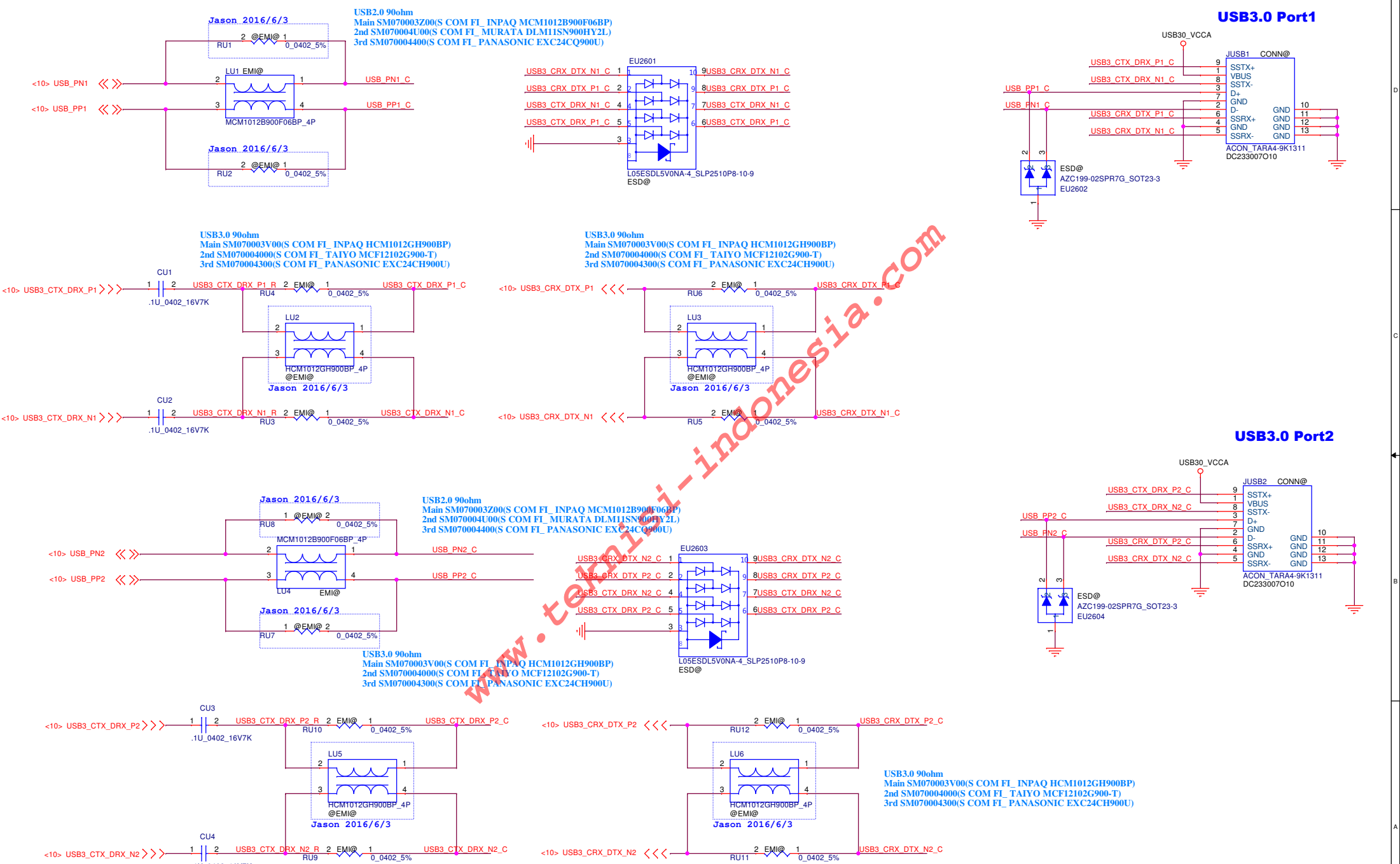
Main Func = Audio Jack



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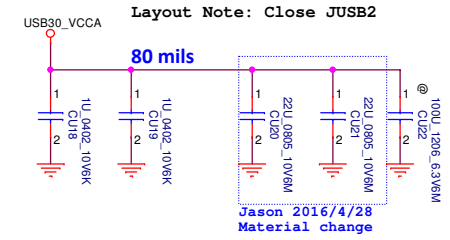
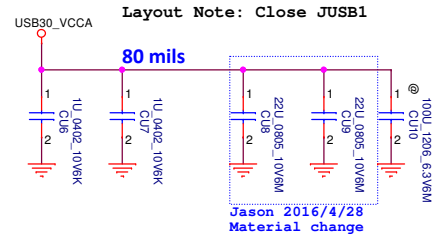
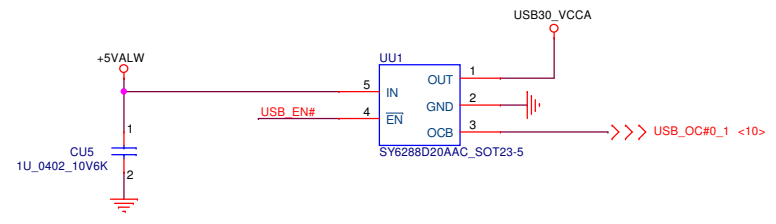
Main Func = USB3.0 Port1



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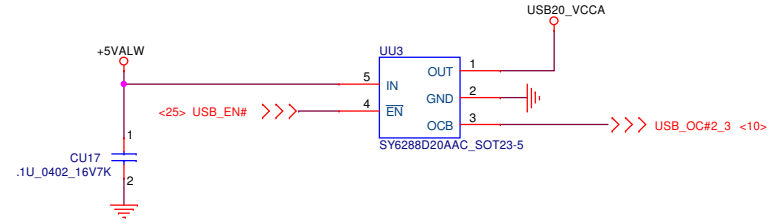
Main Func = USB3.0 Port1/Port2

SY6288D Support 2A

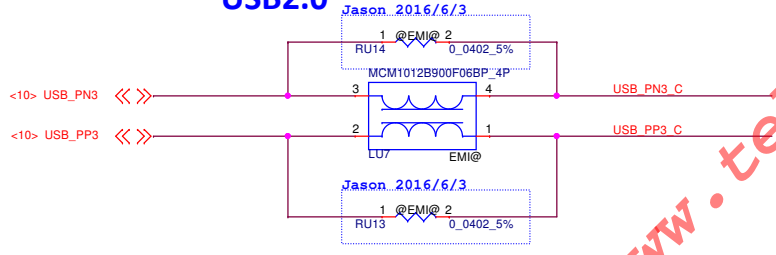


Main Func = USB3.0 Port3

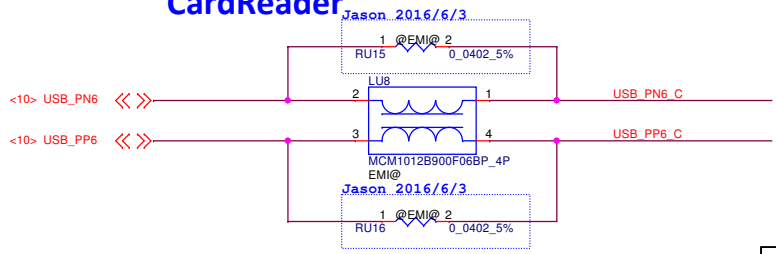
SY6288D Support 2A



USB2.0

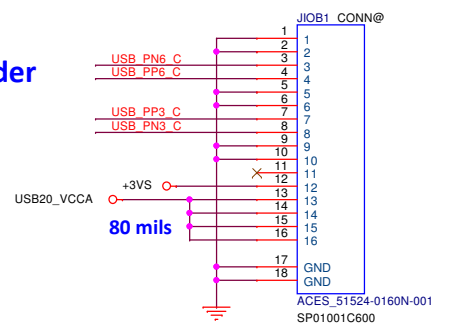


CardReader



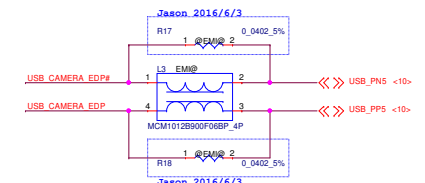
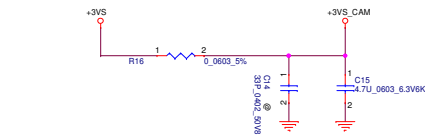
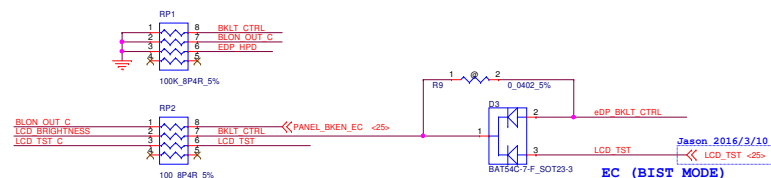
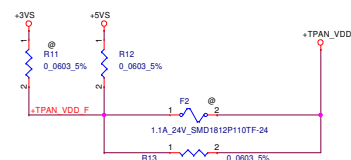
I/O Board Connector

CardReader
USB2.0

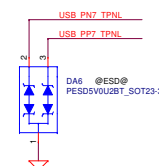
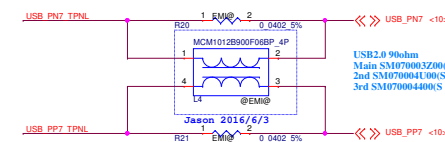
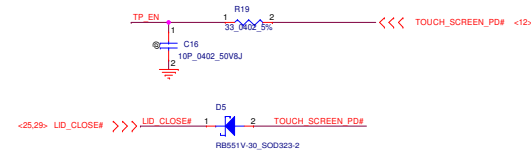


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Size		Document Number			Rev
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Main Func = CAM

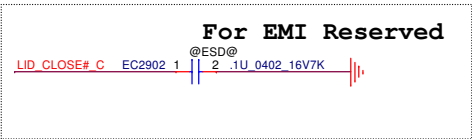
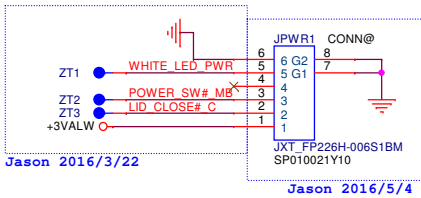
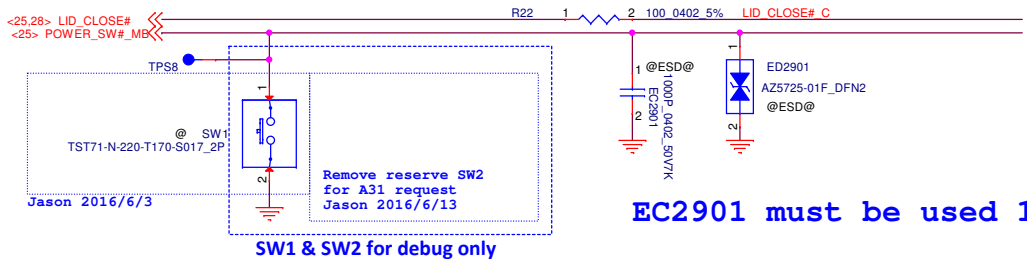


Touch Panel



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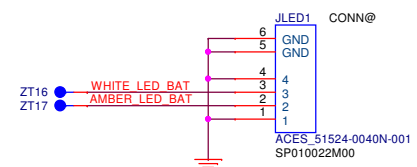
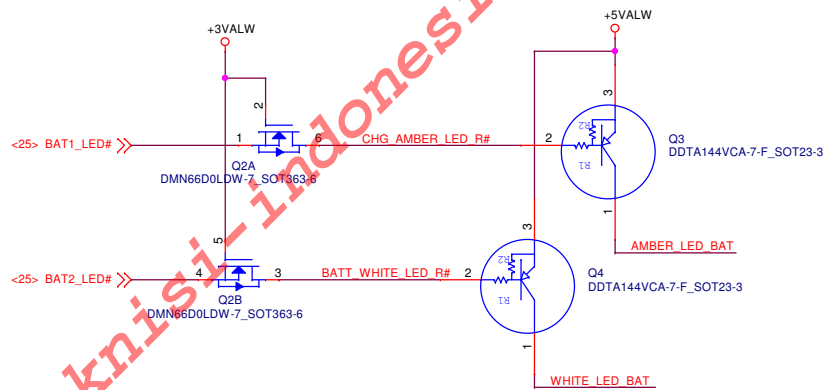
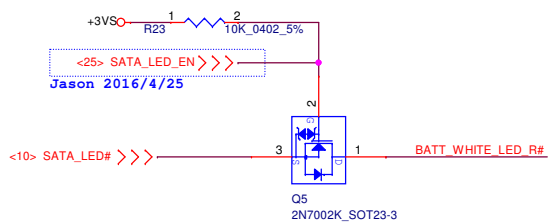
Main Func = Power BTN



Main Func = Battery LED

Low actived from KBC GPIO

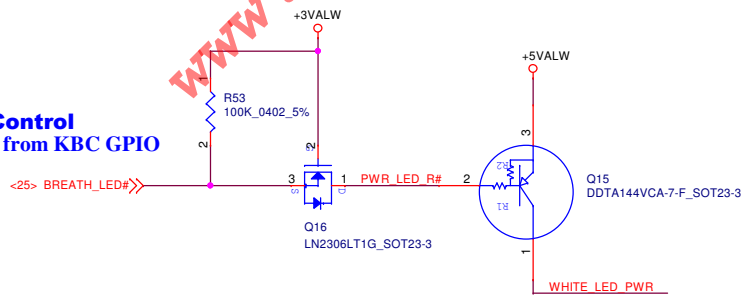
BJT
R1: 47 K
R2: 10 K



Main Func = PWR LED

Low actived from KBC GPIO

PWR LED Control
LOW actived from KBC GPIO



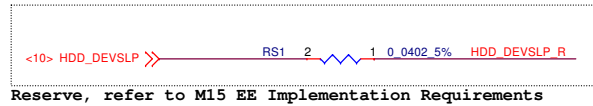
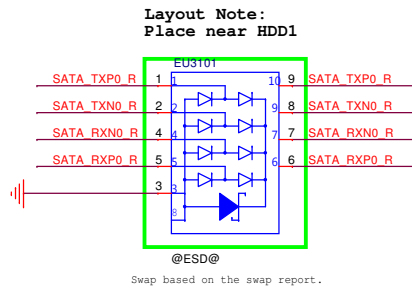
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Issued Date	2016/06/21	Deciphered Date	2017/06/30	Title	
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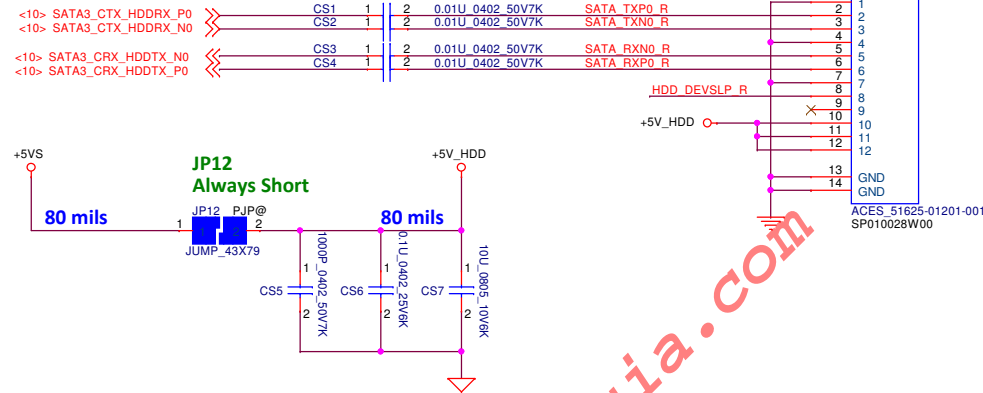
Main Func = HDD

SATA HDD Connector

CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

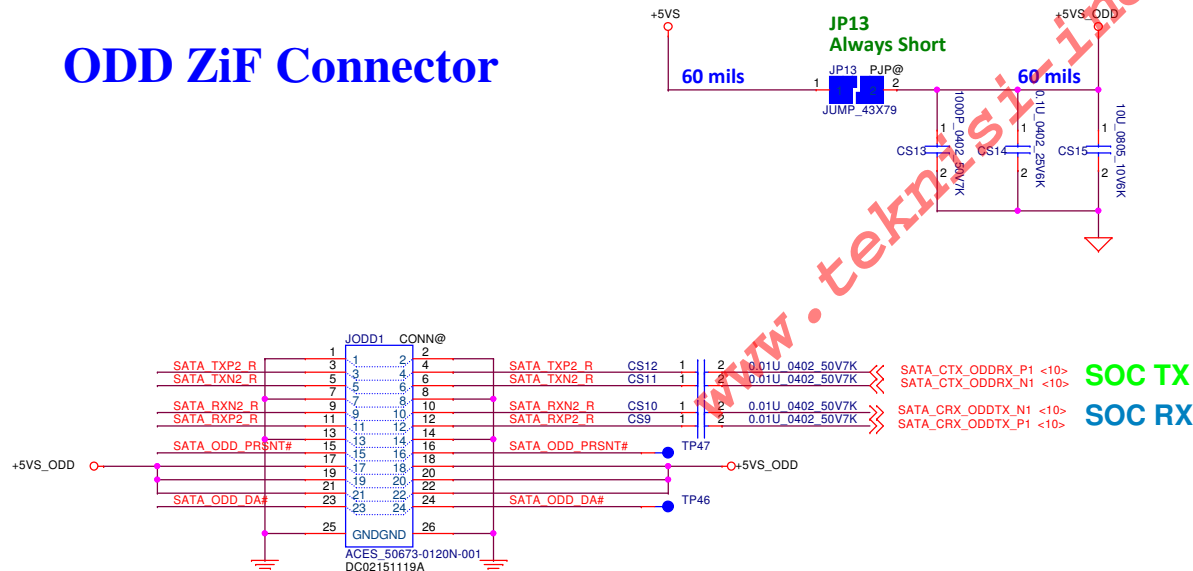


SOC TX
SOC RX



Main Func = ODD

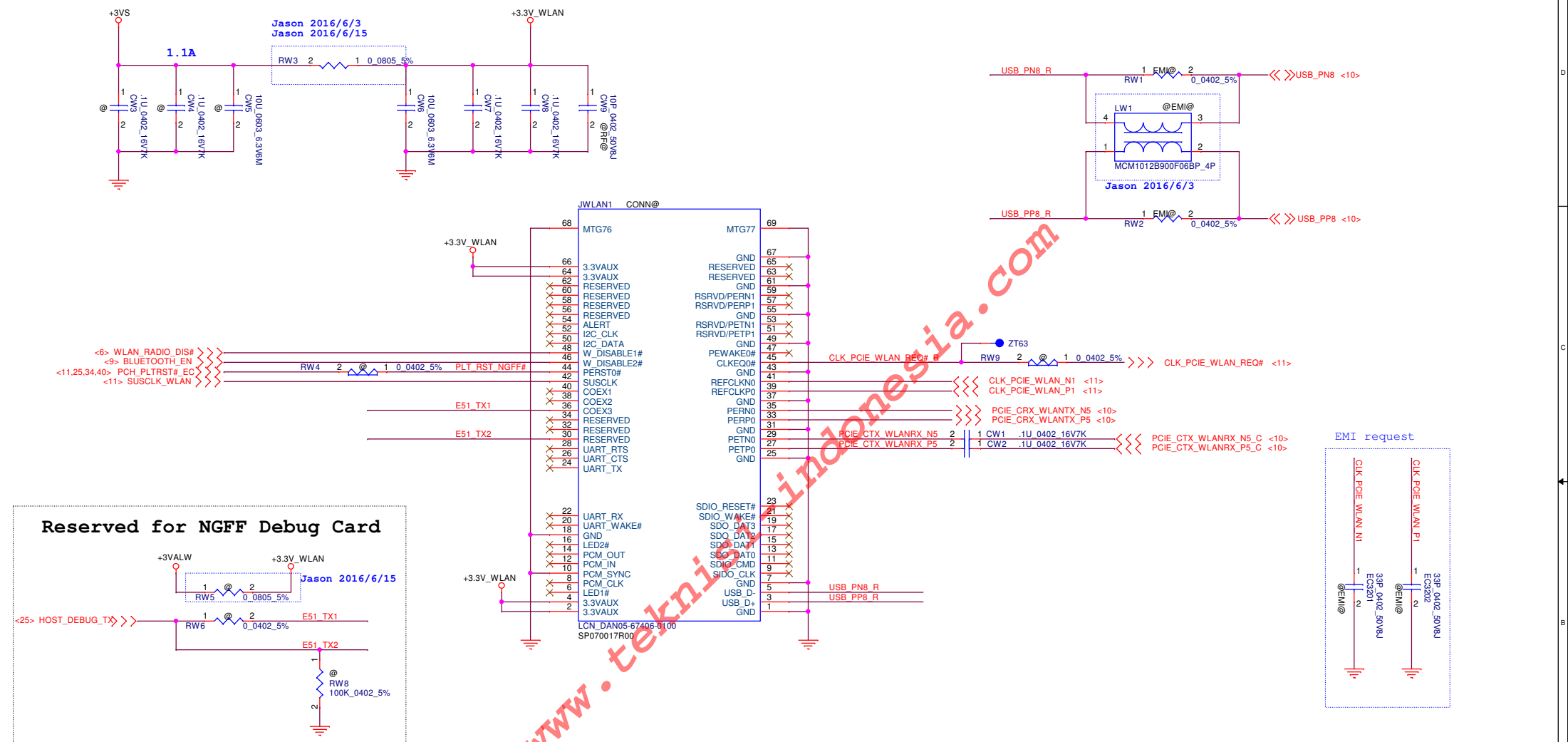
ODD ZiF Connector



Pin	Signal
1	GND
2	A+
3	A-
4	GND
5	B-
6	B+
7	GND
8	DP
9	+5V
10	+5V
11	MD
12	GND
13	GND

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				Date:	Tuesday, June 21, 2016	Sheet 31 of 51

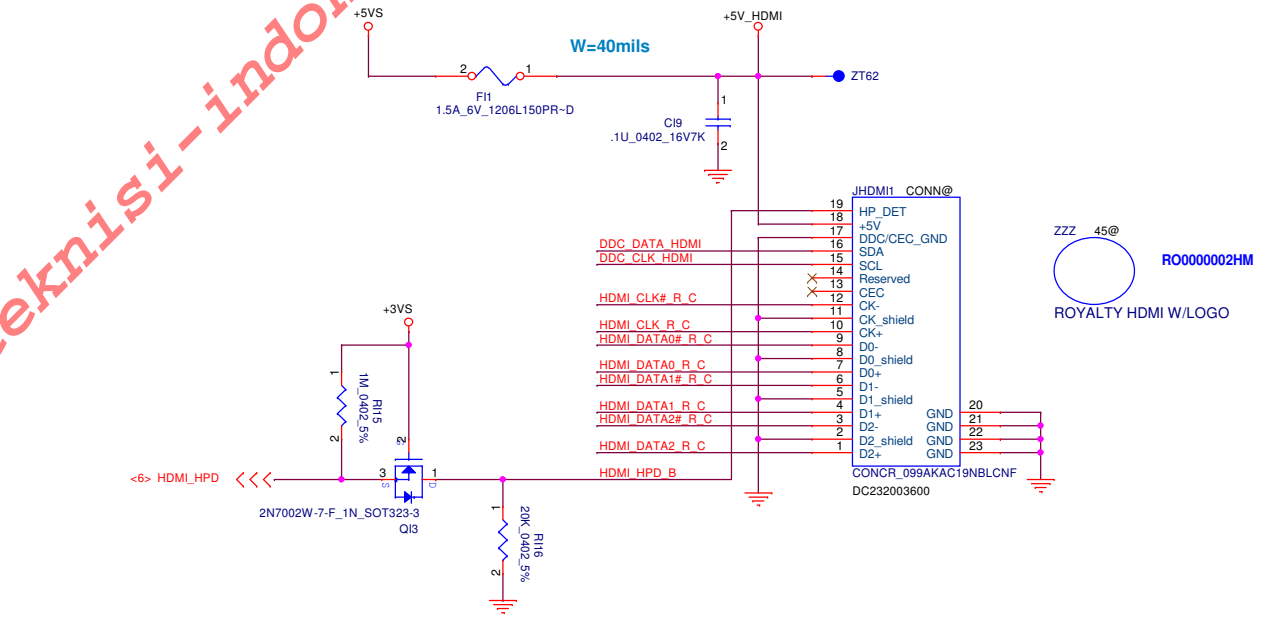
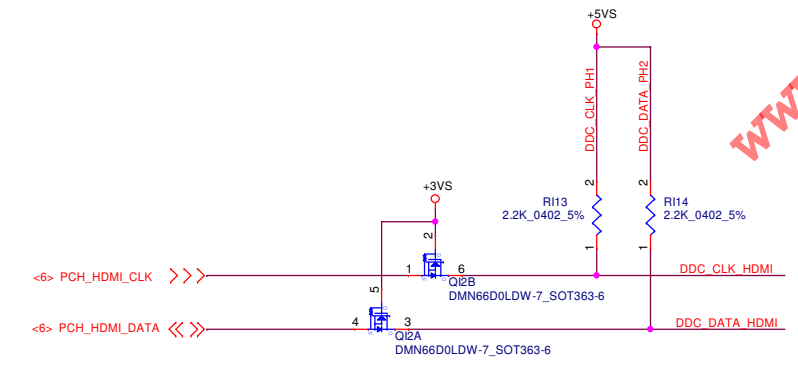
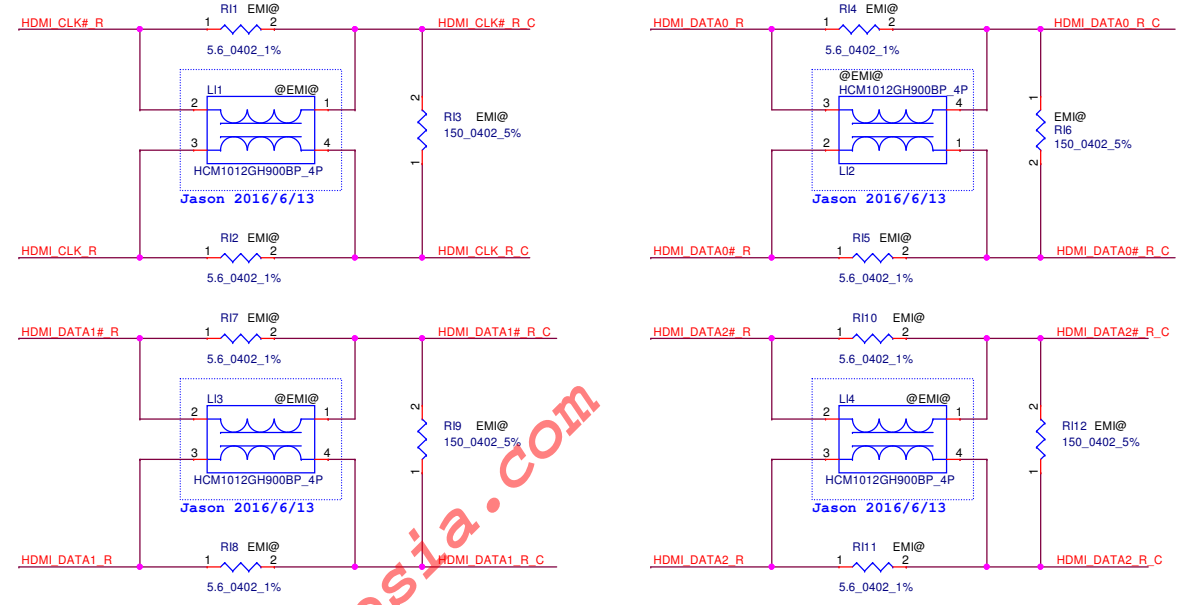
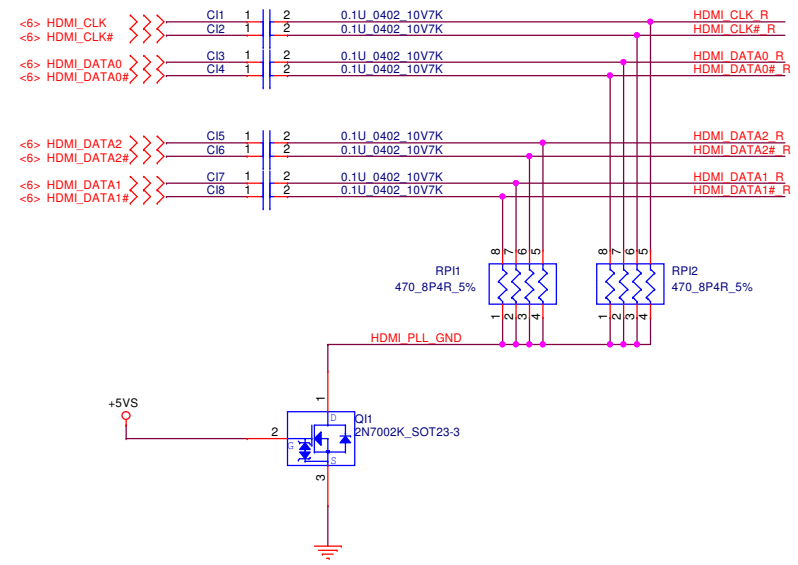
Main Func = WLAN A Key CONN



Support: Intel Dual Band Wireless-AC 3160

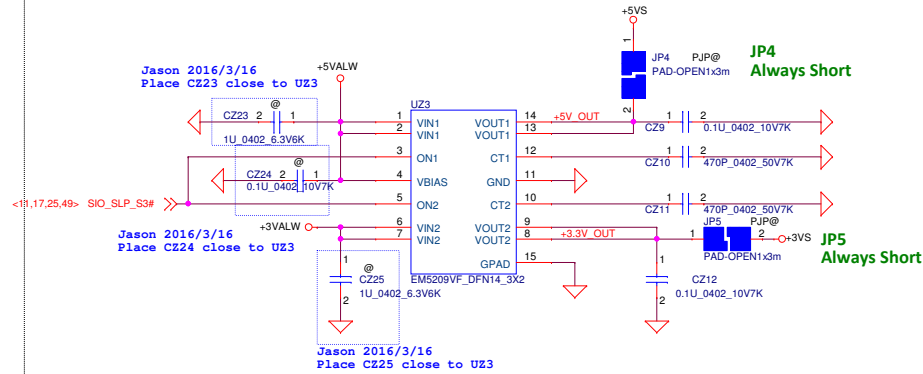
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					NGFF WLAN CONN
					Size Document Number
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Main Func = HDMI

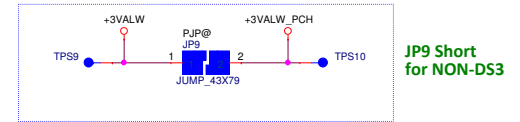


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+5VS/+3VS for System



+3VALW_PCH for System



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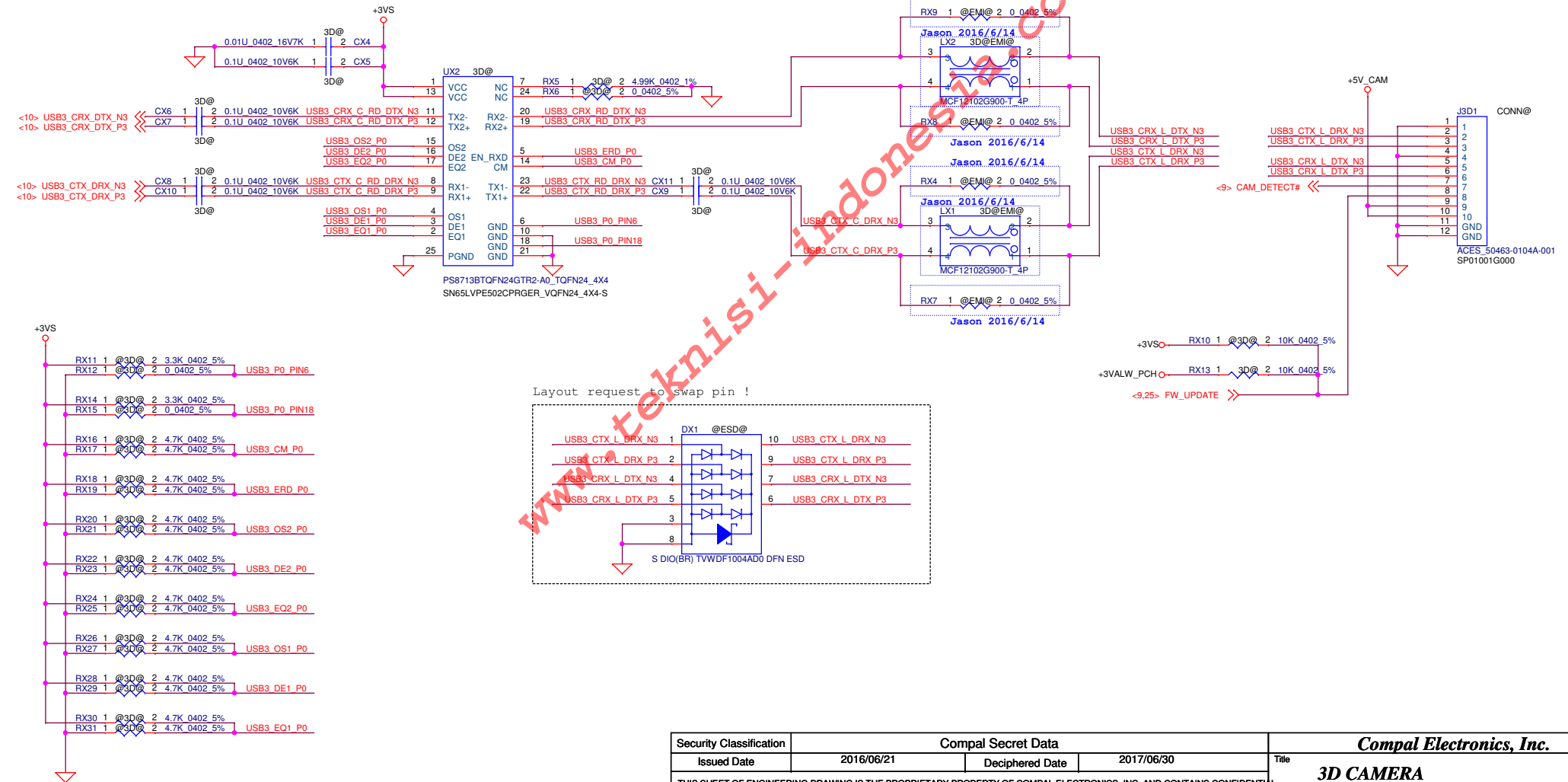
Compal Electronics, Inc.



Title		DC to DC	
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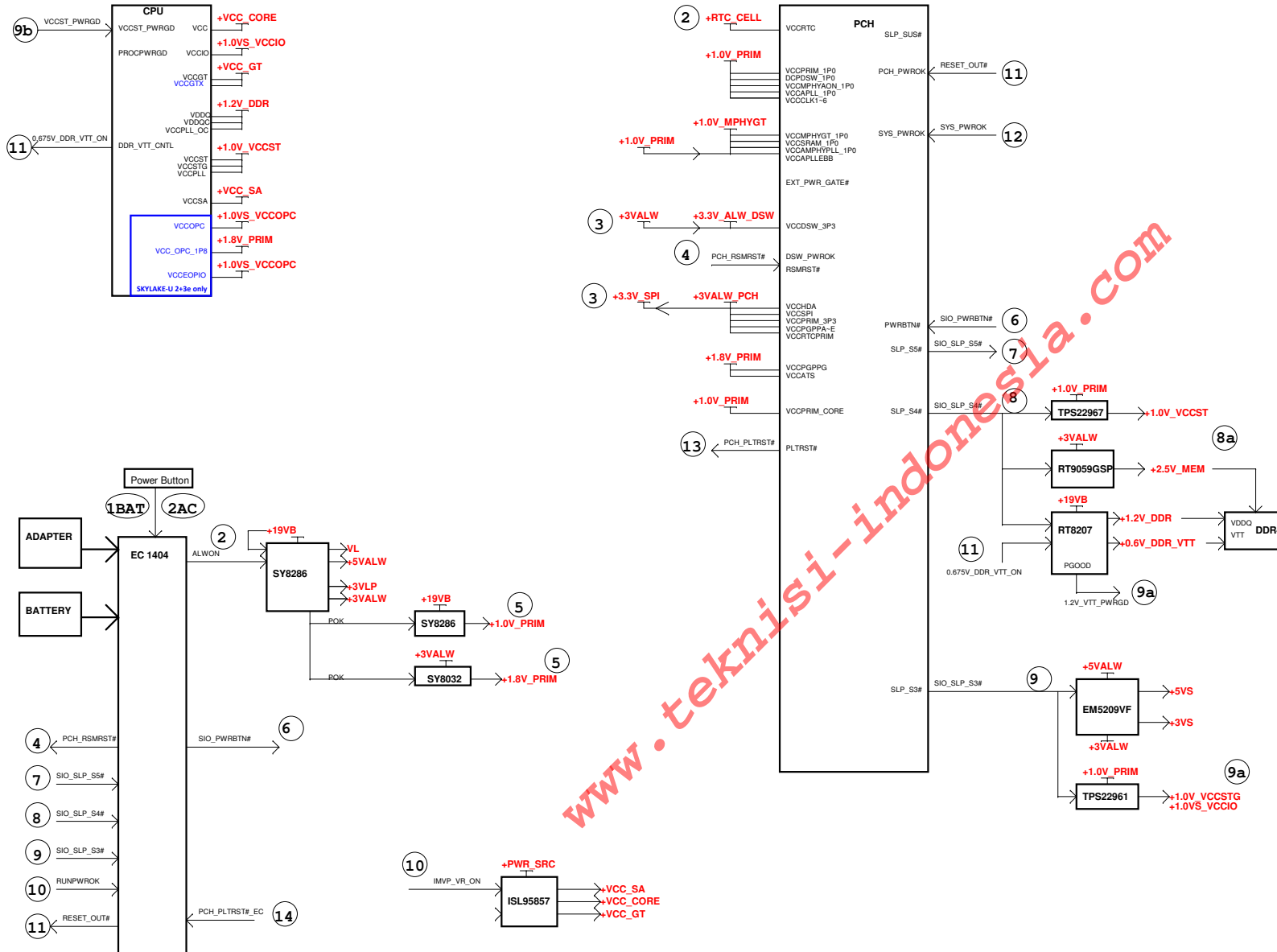
Rev A00

Vendor	PS8713B	TI	Spec	schematic netname	3Vs	GND
1	VDD	VCC	Same			
2	B_EQ0	EQ1	LL: 9.5dB (default) LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_EQ1_P0	RI23	@ RI32
3	DE0	DE1	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE1_P0	RI26	@ RI35
4	EQ1	OS1	LL: 9.5dB LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_OS1_P0	RI22	@ RI40
5	PD#	EN_RXD	it can be left open	USB3_ERD_P0	RI44	@ RI48
6	B_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN6	RI53	@ RI49
7	REXT	NC	4.99K			RI56 4.99K
8	B_Iin	RI1	Same			
9	B_Iin	RI2	Same			
10	GND	GND	Same			
11	A_OUTa	TX2	Same			
12	A_OUTp	TX2+	Same			
13	VDD	VCC	Same			
14	TST/NC	CM	4.7K ohm resistor for performance adjustment	USB3_CM_P0	RI42	@ RI46
15	A_EQ1	OS2	LL: 9.5 dB (default) LH: 13 dB HL: 2.7dB HH: 5 dB	USB3_OS2_P0	RI19	@ RI87
16	A_DE0	DE2	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE2_P0	RI20	@ RI31
17	A_EQ0	EQ2	LL: 9.5 dB (default) LH: 13 dB HL: 2.7dB HH: 5 dB	USB3_EQ2_P0	RI21	@ RI36
18	A_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN18	RI52	@ RI50
19	A_Iin	RI2+	Same			
20	A_Iin	RI2	Same			
21	GND	GND	Same			
22	B_OUTp	TX1+	Same			
23	B_OUTa	TX1	Same			
24	I2C_EN	NC	this pin can be NC or connected to GND	NC		RI57



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Timing Diagram for S5 to S0 mode

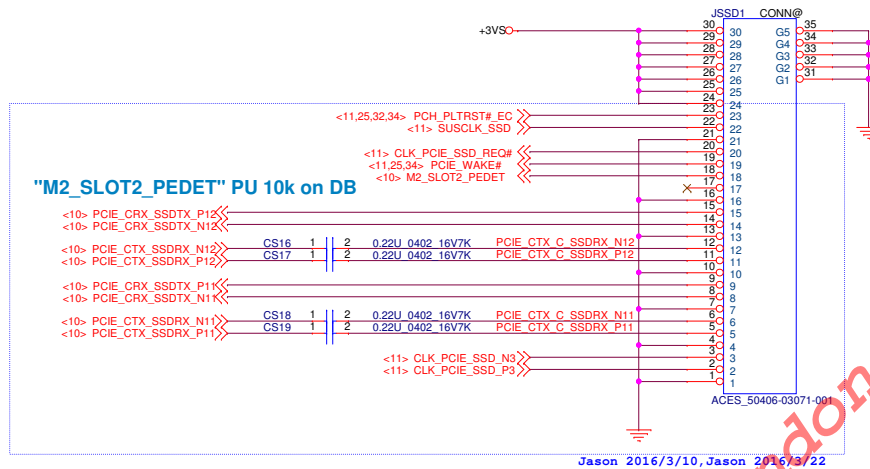


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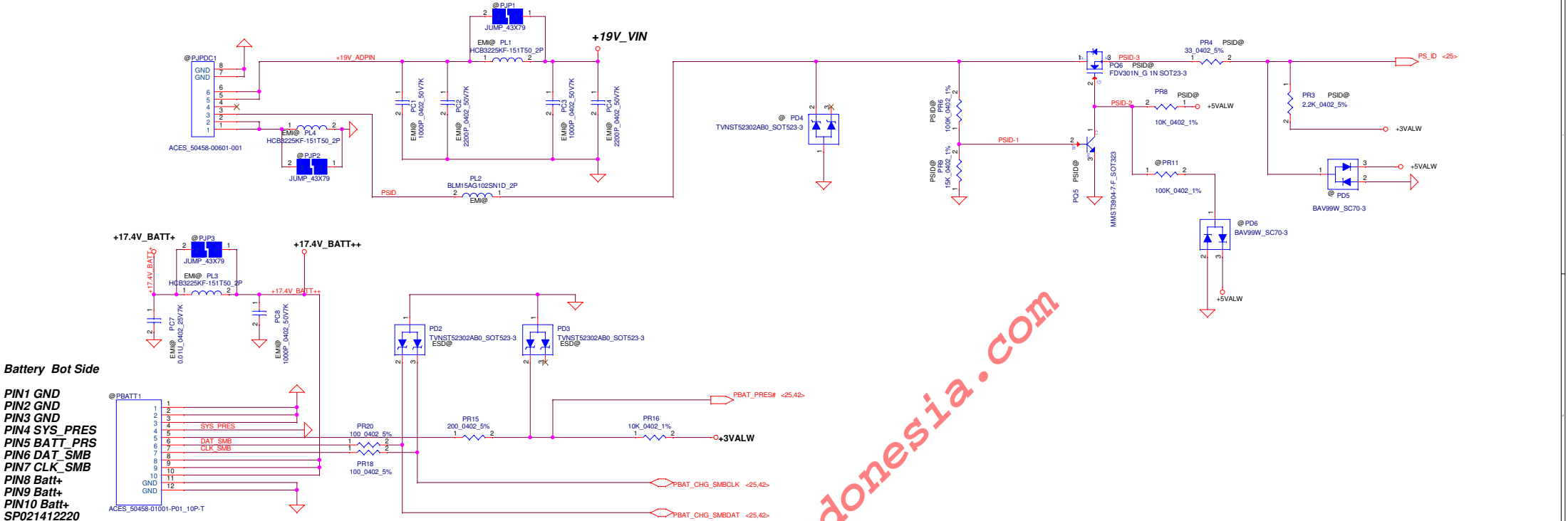
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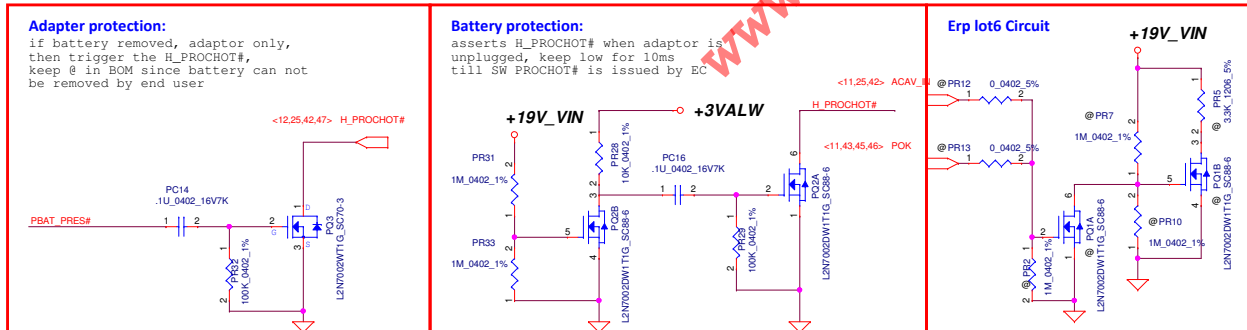
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						Rev A00			



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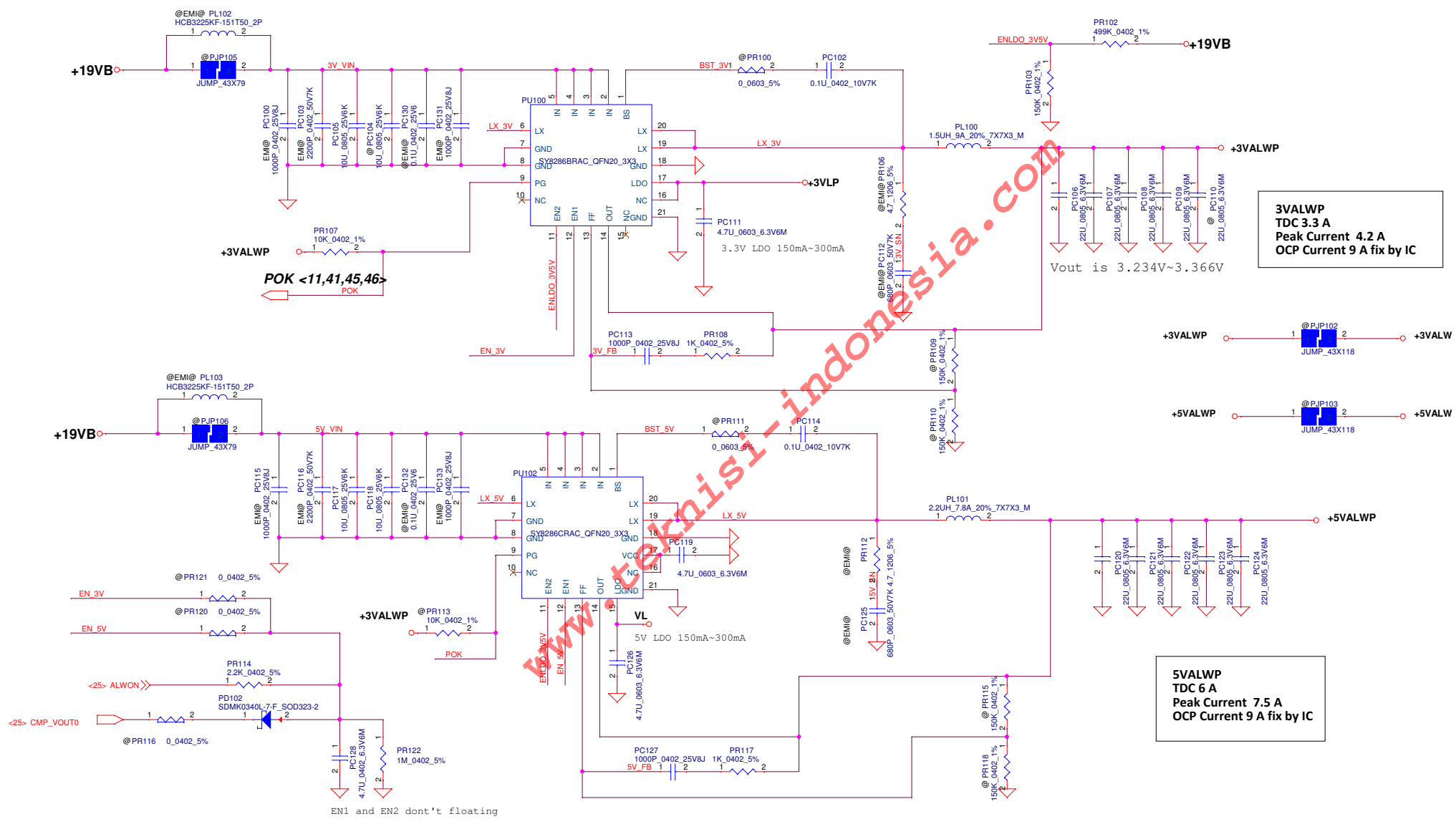
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I_{ada}=0~2.30A (45W)

3S1P: CV = 13.05V CC: 1.9A




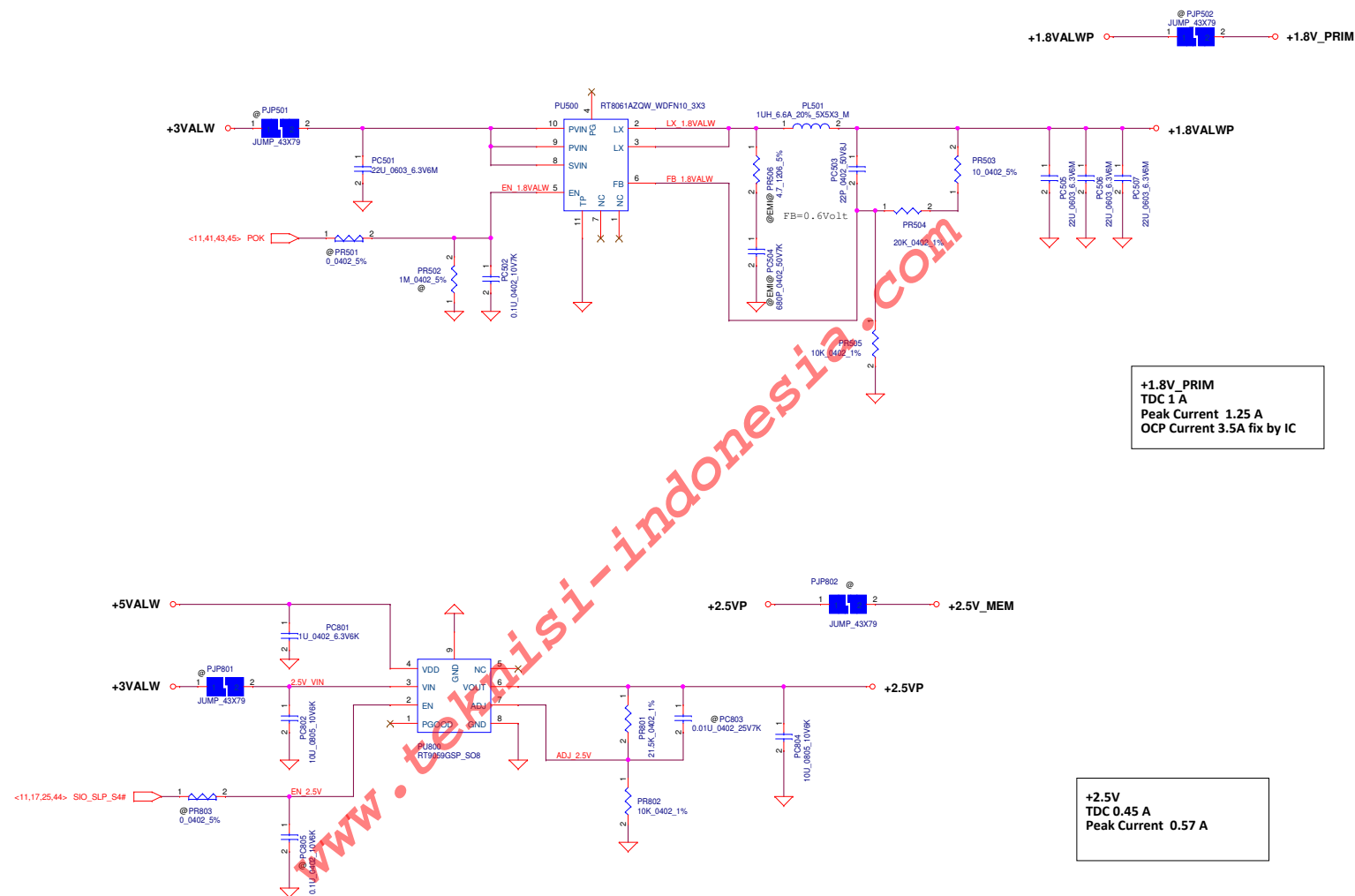
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Title			
PWR 3.3VALWP/5VALWP			
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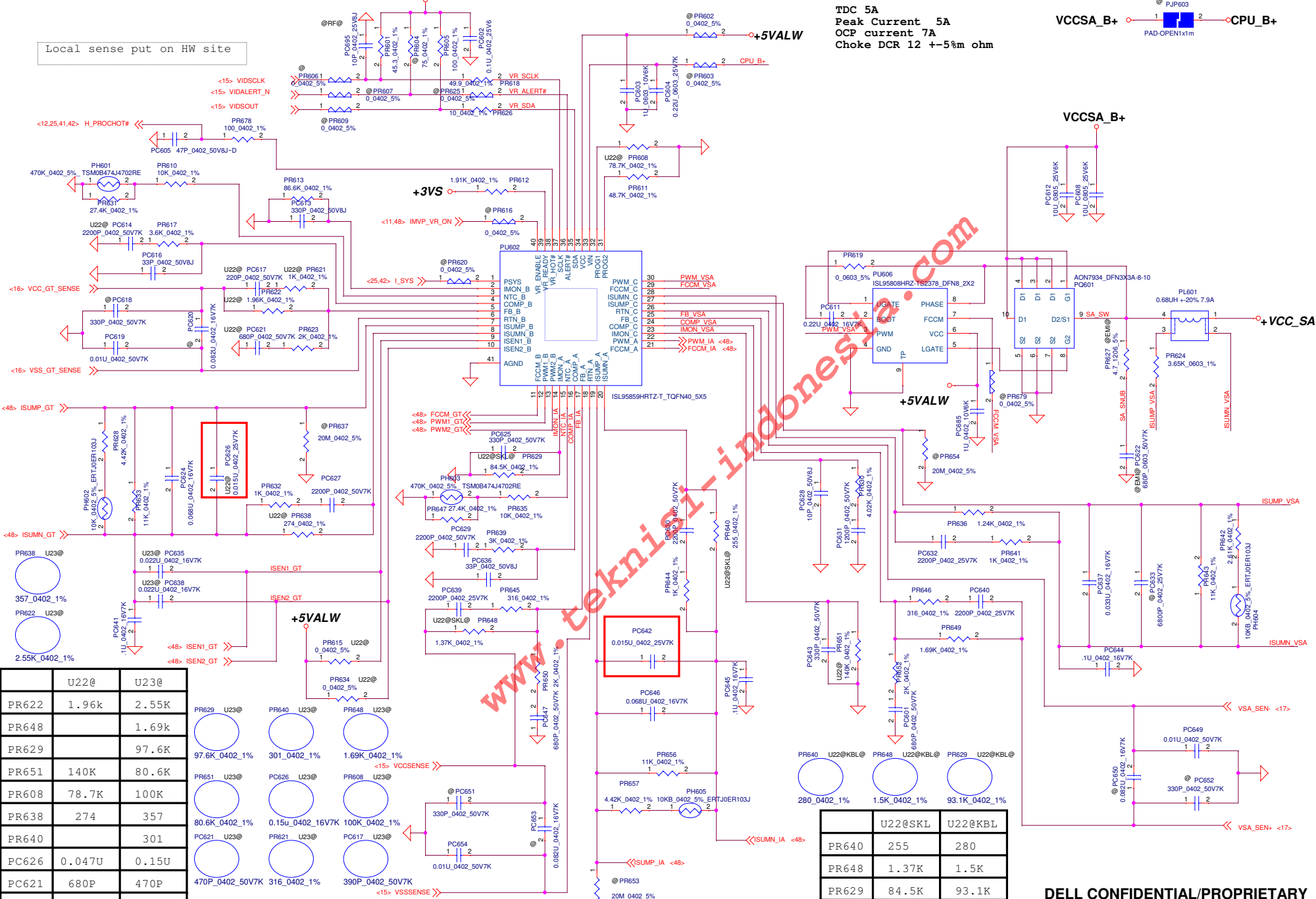
Local sense put on HW site

+1.0V_VCCST

VCC_SA
Loadline : 10.3m-ohm

TDC 5A
Peak Current 5A
OCP current 7A
Choke DCR 12 +-5% m ohm

VCCSA_B+ CPU_B+
PAD-OPEN1x1m



	U22@	U23@
PR622	1.96k	2.55K
PR648		1.69k
PR629		97.6K
PR651	140K	80.6K
PR608	78.7K	100K
PR638	274	357
PR640		301
PC626	0.047U	0.15U
PC621	680P	470P
PR621	1K	316
PC617	220P	390P
PC614	2200P	6800P

Local sense put on HW site

	U22@SKL	U22@KBL
PR640	255	280
PR648	1.37K	1.5K
PR629	84.5K	93.1K

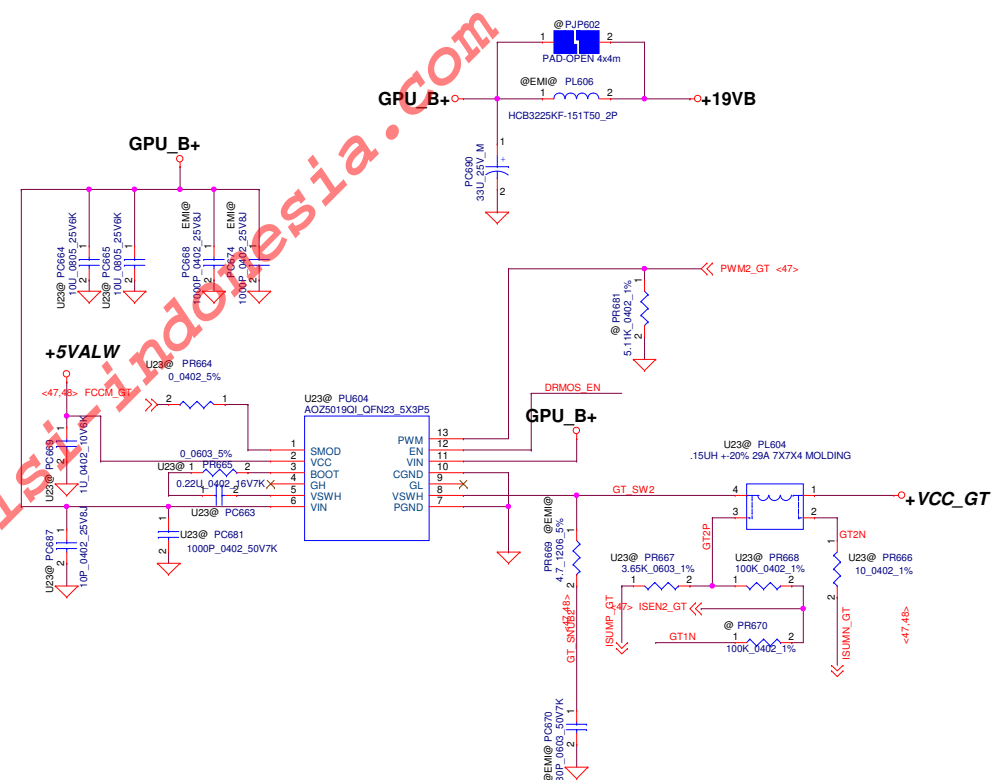
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```
VCC_GT
U22 - 15W
Loadline : 3.1m-ohm
U23e - 15W
Loadline : 2m-ohm
```

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7% ohm

U23e-15W
TDC 43A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7% ohm

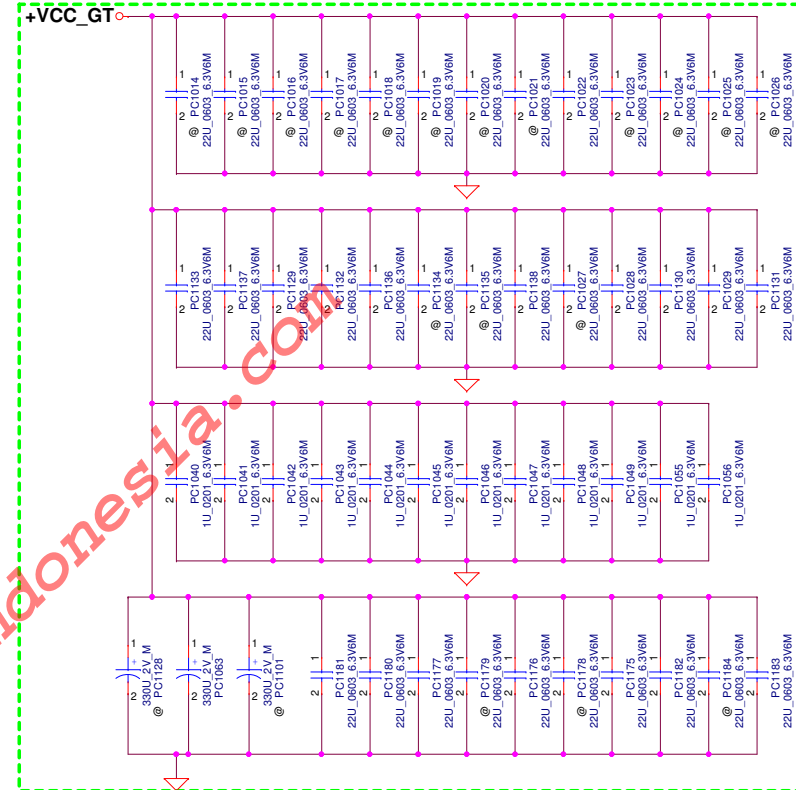


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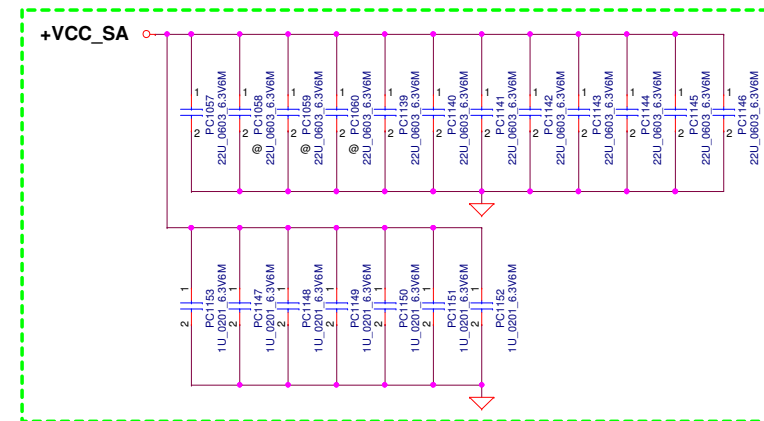
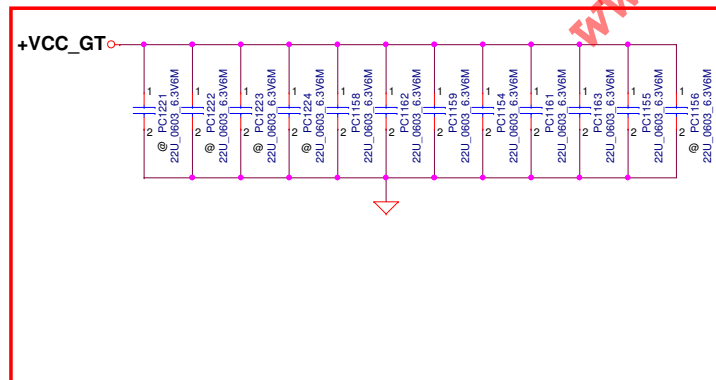
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						Document Number
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KBL :
VCC_CORE Place on CPU
Back Side.
22U_0603 * 15 pcs +1U_0201 *35 pcs
Primary Side.
22U_0603 * 5 pcs+330u *2 pcs

VCC_GT Place on CPU
Back Side.
22U_0603 * 19 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 6 pcs +330u*1 pcs



VCC_SA Place on CPU
Back Side.
22U_0603 * 6 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 3 pcs



Compal Electronics, Inc.

PWR_CPU&VGA bulk and MLCC

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For GTX

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P42	PWR	20150422	COMPAL	design change charger IC	PU706 change to ISL88739 PR732 change to 53.6K PR774 change to 1K PC748 change to 0.1U delete PR727	0.1 (X00)
2	P47	PWR	20150422	COMPAL	design change for IA_Core Iccmax 32A	Change the PR640 to 280 Ohm Change the PR648 to 1.5k Change the PR629 to 93.1k Change the PC642 to 0.01uF Change the PC646 to 0.068uF Change the PC626 to 0.01uF Change the PC624 to 0.068uF	0.1 (X00)
3	P50	PWR	20150422	COMPAL	design change	delete PC1002,PC1003,PC1004,PC1006,PC1012,PC1013,PC1014,PC1015,PC1016,PC1017,PC1018,PC1019,PC1020,PC1021,PC1023,PC1024,PC1025,PC1026,PC1027,PC1058,PC1059,PC1060,PC1068,PC1069,PC1071,PC1072,PC1073,PC1074,PC1075,PC1078,PC1080,PC1081,PC1134,PC1135,PC1156,PC1206,PC1207,PC1208,PC1221,PC1222,PC1223,PC1224 add PC1170,PC1171,PC1172,PC1175,PC1176,PC1177,PC1180,PC1181,PC1182,PC1183	0.1 (X00)
4	P41	PWR	20160504	COMPAL	Reserve Erp lot6	Reserve PR2,PR5 ,PR7,PR10,PQ1	0.3 (X02)
5	P42	PWR	20160504	COMPAL	PQ740 damage issue	Change PQ740 to SB00000SY00 (MDU1512R)	0.3 (X02)
6	P42~P49	PWR	20160504	COMPAL	EMI solution	Change to SE068102J80 (1000P) Location : PC780,PC781,PC100,PC131,PC115,PC133,PC230,PC231,PC694,PC691,PC692,PC693,PC1420,PC1421	0.3 (X02)
7	P42	PWR	20160614	COMPAL	Change SOT23-6P to SOT23-3P	change PQ709 to SB00000ST00 (PQ709,PQ712)	1.0 (A00)
8	P42	PWR	20160614	COMPAL	Add pull high resistance	Add PR781	1.0 (A00)

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